ADSP-21364 EZ-KIT Lite®
Evaluation System Manual

Revision 2.0, January 2005

Part Number
82-000840-01

Analog Devices, Inc.
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Norwood, Mass. 02062-9106

ANALOG DEVICES

Copyright Information

Printed in the USA.

Limited Warranty

The EZ-KIT Lite evaluation system is warranted against defects in materials and workmanship for a period of one year from the date of purchase from Analog Devices or from an authorized dealer.

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Regulatory Compliance

The ADSP-21364 EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the "**CE**" mark.

The ADSP-21364 EZ-KIT Lite evaluation system had been appended to Analog Devices Development Tools Technical Construction File referenced "DSPTOOLS1" dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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CONTENTS

PREFACE

EZ-KIT LITE HARDWARE REFERENCE

PREFACE

Thank you for purchasing the ADSP-21364 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for SHARC® processors.

The SHARC processors are based on a 32-bit super Harvard architecture that includes a unique memory architecture comprised of two large on-chip, dual-ported SRAM blocks coupled with a sophisticated IO processor, which gives a SHARC processor the bandwidth for sustained high-speed computations. SHARC processors represents today's de facto standard for floating-point processor targeted for premium audio applications.

The evaluation system is designed to be used in conjunction with the VisualDSP++® development environment to test the capabilities of the ADSP-21364 SHARC processors. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-21364 assembly
- Load, run, step, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-21364 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-21364 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to `http://www.analog.com/dsp/tools/`.

The ADSP-21364 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-21364 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a users program to 10922 words of internal memory for code space with no restrictions for data space.

ADSP-21364 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

The board features:

- Analog Devices ADSP-21364 processor
  - 136-pin BGA package
  - 300 MHz Core Clock Speed

- Synchronous Random Access Memory (SRAM)
  - 512 Kbit x 8-bit
- Flash Memory
  - 1M x 8-bit
- Serial Peripheral Interconnect (SPI) Flash Memory
  - 512 Kbit
- Analog Audio Interface
  - AD1835A codec
  - 4x2 RCA phono jack for 4 channels of stereo output
  - 2x1 RCA phono jack for 1 channel of stereo input
  - Headphone jack for 1 channel stereo output
- Digital Audio Interface
  - RCA phono jack output
  - RCA phono jack input
- LEDs
  - 12 LEDs: 1 power (green), 1 board reset (red), 1 USB reset (red), 1 USB monitor (amber), and 8 general purpose (amber)
- Push Buttons
  - 5 push buttons: 1 reset, 2 connected to DAI, 2 connected to the `FLAG` pins of the processor

- Expansion Interface (Type A)
  - Parallel Port, FLAGs, DAI, SPI
- Other Features
  - JTAG ICE 14-pin header
  - 0-ohm resistors for processor current measurement
  - SPI header
  - DAI header

The EZ-KIT Lite board has a total of 1 MB of parallel flash memory and 512 Kbit of SPI flash memory. The flash memories can store user-specific boot code, allowing the board to run as a stand-alone unit. For more information, see "External Memory" on page 1-6 and "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11. The board also has 512 KB of SRAM, which can be used at runtime.

The DAI of the processor connects to the AD1835A audio codec and two connectors, which allow SPDIF input and output. The interface facilitates development of digital and analog audio signal-processing applications. See "Analog Audio" on page 1-7 and "SPDIF Coax Connectors (J8 and J9)" on page 2-18 for more information.

Additionally, the EZ-KIT Lite board provides access to all of the processor's peripheral ports. Access is provided in the form of a three-connector expansion interface. See "Expansion Interface" on page 2-7 for details.

Purpose of This Manual

The *ADSP-21364 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board) and describes the operation and configuration of the board components. The product software component is detailed in the *VisualDSP++ Installation Quick*

Reference Card. The manual provides guidelines for running your own code on the ADSP-21364 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-2136x SHARC Processor Programming Reference* and *ADSP-2136x SHARC Processor Hardware Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and the VisualDSP++ user's or getting started guides. For the locations of these documents, see "Related Documents".

Manual Contents

The manual consists of:

- Chapter 1, "Using EZ-KIT Lite" on page 1-1
  Provides information on the EZ-KIT Lite from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the hardware aspects of the evaluation system.

- Appendix A, "Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "Schematics" on page B-1
  Provides the resources to allow modifications to the EZ-KIT Lite or to use as a reference design.

This appendix is not part of the online Help. The online Help viewers should go to the PDF version of the ADSP-21364 EZ-KIT Lite Evaluation System Manual located in the `Docs\EZ-KIT Lite Manuals` folder on the installation CD to see the schematics. Alternatively, the schematics can be found on the Analog Devices Web site, `www.analog.com/processors`.

What's New in This Manual

This revision of the *ADSP-21364 EZ-KIT Lite Evaluation System Manual* provides an updated listing of related documents and updated licensing information.

Technical or Customer Support

You can reach DSP Tools Support in the following ways.

- Visit the Embedded Processing and processor products Web site at `http://www.analog.com/processors/technicalSupport`
- E-mail tools questions to `dsptools.support@analog.com`
- E-mail processor questions to `dsp.support@analog.com`
- Phone questions to **1-800-ANALOGD**

- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:

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Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
USA
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Supported Processors

The ADSP-21364 EZ-KIT Lite evaluation system supports the Analog Devices ADSP-21364 SHARC processors.

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at `www.analog.com`. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and processors, visit our Web site at www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
  dsp.support@analog.com
- Fax questions or requests for information to
  1-781-461-3010 (North America)
  +49 (89) 76 903-557 (Europe)
- Access the FTP Web site at
  ftp ftp.analog.com or ftp 137.71.23.21
  ftp://ftp.analog.com

Related Documents

For information on product related development software and hardware, see these publications:

Table 1. Related Processor Publications

Title	Description
ADSP-21364 SHARC Microprocessor Datasheet	General functional description, pinout, and timing
ADSP-2136x SHARC Processor Hardware Reference	Description of internal processor architecture, registers, and all peripheral functions
ADSP-2136x SHARC Processor Programming Reference	Description of all allowed processor assembly instructions

Table 2. Related VisualDSP++ Publications

VisualDSP++ User's Guide	Detailed description of VisualDSP++ features and usage
VisualDSP++ Assembler and Preprocessor Manual	Description of the assembler function and commands
VisualDSP++ C/C++ Complier and Library Manual for SHARC Processors	Description of the complier function and commands for SHARC processors
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands
VisualDSP++ Loader Manual	Description of the loader function and commands

If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

`http://www.analog.com/processors/resources/technicalLibrary`

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary `.PDF` files of most manuals are provided in the `Docs` folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

File	Description
`.CHM`	Help system files and manuals in Help format
`.HTM` or `.HTML`	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the `.HTML` files requires a browser, such as Internet Explorer 4.0 (or higher).
`.PDF`	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the `.PDF` files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows® Explorer, or the Analog Devices Web site.

Accessing Documentation From VisualDSP++

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and navigate to the VisualDSP++ documentation via the **Start** menu.

To view ADSP-21364 EZ-KIT Lite Help,which is part of the VisualDSP++ Help system, use the **Contents** or **Search** tab of the Help window.

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (`.CHM`) are located in the `Help` folder, and `.PDF` files are located in the `Docs` folder of your VisualDSP++ installation CD-ROM. The `Docs` folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Your software installation kit includes online Help as part of the Windows® interface. These help files provide information about VisualDSP++ and the ADSP-21364 EZ-KIT Lite evaluation system.

Accessing Documentation From Web

Download manuals at the following Web site:
`http://www.analog.com/processors/resources/technicalLibrary/manuals`.

Select a processor family and book title. Download archive (`.ZIP`) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call **1-603-883-2430**. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto `http://www.analog.com/salesdir/continent.asp`.

Hardware Tools Manuals

To purchase EZ-KIT Lite and In-Circuit Emulator (ICE) manuals, call **1-603-883-2430**. The manuals may be ordered by title or by product number located on the back cover of each manual.

Processor Manuals

Hardware reference and instruction set reference manuals may be ordered through the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**), or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.

Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**); they also can be downloaded from the Web site.

To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 USING EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-21364 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "Example Programs" on page 1-10
  Provides information about the example programs included in the ADSP-21364 EZ-KIT Lite evaluation system.
- "Background Telemetry Channel" on page 1-11
  Highlights the advantages of the Background Telemetry Channel feature of VisualDSP++.
- "VisualDSP++ Interface" on page 1-11
  Describes the boot loading, target options, and other facilities of the EZ-KIT Lite system.

For detailed information on how to program the ADSP-21364 SHARC processor, refer to the documents referenced in "Related Documents" on page -xvi.

Package Contents

Your ADSP-21364 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-21364 EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*
- CD containing:
  - VisualDSP++ software
  - ADSP-21364 EZ-KIT Lite debug software
  - USB driver files
  - Example programs
  - *ADSP-21364 EZ-KIT Lite Evaluation System Manual* (this document)

- Universal 7.5V DC power supply
- USB 2.0 cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-21364 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components.

To connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package. Be careful when handling the board to avoid the discharge of static electricity, which may damage some components.

2. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before continuing.

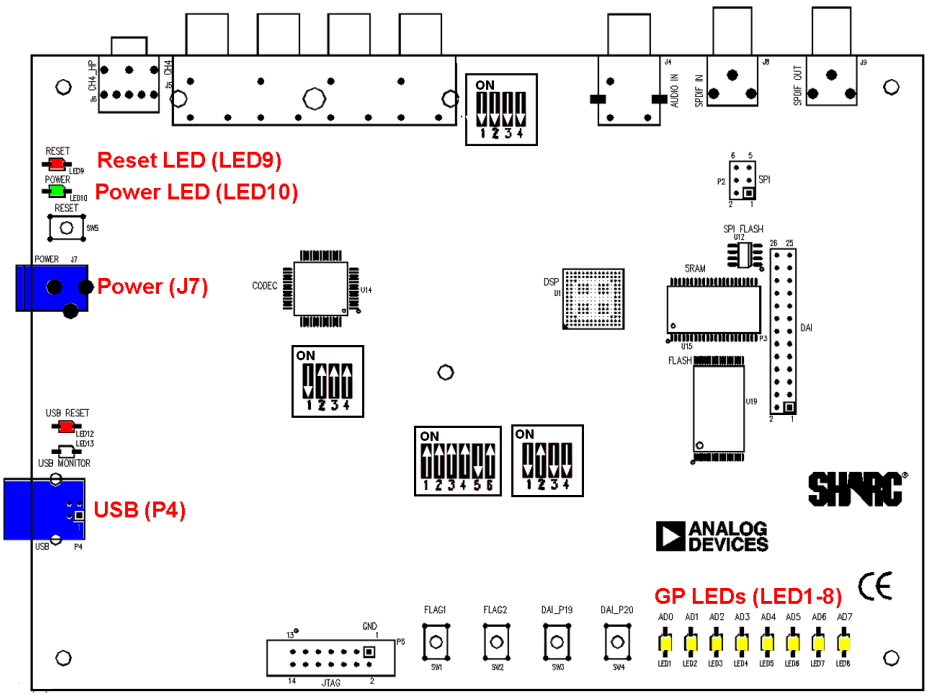

Figure 1-1. EZ-KIT Lite Hardware Setup

3. Plug the provided power supply into J7 on the EZ-KIT Lite board. Visually verify that the green power LED (LED10) is on. Also verify that the two red reset LEDs (LED9 and LED12) go on for a moment and then go off, and, finally, LED8-1 are continually blinking.
4. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to P4 on the ADSP-21364 EZ-KIT Lite board.

Installation and Session Startup

For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

To start up an EZ-KIT Lite session in VisualDSP++:

1. Verify that the yellow USB monitor LED (LED13, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. From the **Start** menu, navigate to the VisualDSP++ environment via the **Programs** menu.
   If you are running VisualDSP++ for the first time, the **New Session** dialog box appears on the screen (skip the rest of the procedure and go to step 3).
   If you have run VisualDSP++ previously, the last opened session appears on the screen.
   To switch to another session, via the **Session List** dialog box, hold down the **Ctrl** key while starting VisualDSP++ (go to step 5).
3. In **Debug target,** select **EZ-KIT Lite** (**ADSP-21xxx**).
   In **Platform**, select **ADSP-21xxx EZ-KIT Lite**.
   In **Processor**, choose the appropriate processor, **ADSP-21364**.
   In **Session name**, type a new name or accept the default.

4. Click **OK** to return to the **Session List**.
5. Highlight the session and click **Activate**.

Evaluation License Restrictions

The ADSP-21364 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

1. VisualDSP++ allows a connection to the ADSP-21364 EZ-KIT Lite via the USB Debug Agent interface only. Connections to simulators and emulation products are no longer allowed.
2. The linker restricts a users program to 10922 words of internal memory for code space with no restrictions for data space.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

External Memory

The EZ-KIT Lite contains three types of memory: parallel flash (1 MB), SPI flash (512 Kbit) and SRAM (512 Kbit). The flash memories can store user-specific boot code, letting the board to run as a stand-alone unit. For more information about setting the boot device for the processor, see "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11.

Table 1-1 provides a map of the board's external memory.

The parallel flash memory and the SRAM connect to the parallel port of the processor. The parallel port is a multiplexed address and data port. The port can connect to 8-bit and 16-bit memory devices. When configuring the parallel port, keep in mind that the memory devices on the board are 8 bits wide.

Table 1-1. EZ-KIT Lite Evaluation Board External Memory

Start Address	End Address	Content
0x0100 0000	0x010F FFFF	Flash memory
0x0120 0000	0x0127 FFFF	SRAM memory
0x0140 0000	0x0140 FFFF	LEDs (see "LEDs and Push Buttons" on page 2-12)
0x0160 0000	0x017F FFFF	Unused chip select 1
0x0180 0000	0x019F FFFF	Unused chip select 2

To access the SRAM and flash memories, set up a Parallel Port DMA. For more information on how to connect the SRAM and flash memories, see "Parallel Port" on page 2-3.

The SPI flash memory connects to the SPI port of the processor and uses `Flag0` as a chip select. In order for `FLAG0` to behave as a chip select, clear the `PPFLG` bit in the `SYSCLT` register.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how the parallel port and SPI port can be configured to access the memories.

Analog Audio

The AD1835A is a high-performance, single-chip codec featuring four stereo digital-to-analog converters (DAC) for audio output and one stereo analog-to-digital converters (ADC) for audio input. The codec can input and output data with a sample rate of up to 96 kHz on all channels. A 192 kHz sample rate can be used with the one of the DAC channels.

The processor is interfaced with the AD1835A via the DAI port. The DAI interface pins can be configured to transfer serial data from the AD1835A codec in either Time-Division Multiplexed (TDM) or Two-Wire Interface mode. For more information on how the AD1835A connects to the DAI, see "DAI Interface" on page 2-5.

The master input clock (MCLK) for the AD1835A can be generated by the on-board 12.288 MHz oscillator or can be supplied by one of the DAI pins of the processor. Using one if the pins to generate the MCLK, as opposed to the on-board oscillator, allows synchronization of multiple devices in the system. This is done on the EZ-KIT Lite when data is coming from the SPDIF receiver and being output through the audio codec. The SPDIF MCLK is routed to the AD1835A MCLK in the processor's SRU. It is also necessary to disable the on-board audio oscillator from driving the audio codec and the processor's input pin. For instructions on how to configure the clock, refer to "Codec Setup Switch (SW7)" on page 2-8.

The AD1835A codec can be configured as a master or as a slave, depending on DIP switch settings. In master mode, the AD1835A drives the serial port clock and frame sync signals to the processor. In slave mode, the processor must generate and drive all of the serial port clock and frame sync signals. For information on how to set the mode, refer to "Codec Setup Switch (SW7)" on page 2-8.

The AD1835A audio codec's internal configuration registers are configured using the SPI port of the processor. The FLAG3 register is used as the select for the device. For information on how to configure the multichannel codec, refer to the codec datasheet, which can be found at www.analog.com.

The RCA connector (J4) is used to input analog audio. When using an electret microphone on this connector, configure the SW6 switch according the instructions in "Electret Microphone Select Switch (SW6)" on page 2-8. The four output channels connect to the RCA connector J5. Channel 4 of the codec connects to the headphone jack J6. For more information about the connectors see "Connectors" on page 2-15.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to configure and use the board's analog audio interface.

LEDs and Push Buttons

The EZ-KIT Lite has eight general-purpose user LEDs and four general-purpose push buttons.

Two of the general-purpose push buttons are attached to the FLAG pins of the processor, while the other two are attached to the DAI pins. All of the push buttons connect to the processor through a DIP switch. The DIP switch allows processor pins, which connect to the push buttons, to be disconnected. See "Push Button Enable Switch (SW9)" on page 2-10 for instructions on how to disable the push buttons from driving the corresponding processor pin.

The value of the push buttons connected to the FLAG pins can be determined by reading the FLAG register. The push buttons connected to the DAI pins must be configured as interrupts. It is necessary to set up an interrupt routine to determine each pin's state. Table 1-2 shows how each push button connects to the processor. Refer to the related example program shipped with the EZ-KIT Lite for more information.

Table 1-2. Push Button Connections

Push Button Reference Designator	Processor Pin
SW1	FLAG1
SW2	FLAG2
SW3	DAI19
SW4	DAI20

The LEDs are connected to the parallel port pins, AD7-0, via a latch. The parallel port of the processor can be set up as a memory bus or as general-purpose FLAG pins. The latch allows the LEDs to be written to in both cases. Information about setting up the latch can be found in "Push Button Enable Switch (SW9)" on page 2-10.

When the LEDs are accessed as FLAG pins, the latch must be set up to pass the data through to pins AD7-0 of the processor. In this mode, it is also necessary to set up the parallel port to be FLAG pins. To set up the parallel port as FLAG pins, set the PPFLGS bit in the SYSCTL register. Table 1-3 summarizes the LED and FLAG connections.

Table 1-3. LED Connections

LED Reference Designator	Processor Pin	Mapped as FLAG
LED1	AD0	FLAG8
LED2	AD1	FLAG9
LED3	AD2	FLAG10
LED4	AD3	FLAG11
LED5	AD4	FLAG12
LED6	AD5	FLAG13
LED7	AD6	FLAG14
LED8	AD7	FLAG15

An example program is included in the EZ-KIT Lite installation directory to demonstrate the functionality of the LEDs and push buttons.

Example Programs

Example programs are provided with the ADSP-21364 EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in the \…\213xx\EZ-KITs\ADSP-21364\Examples subdirectory of the VisualDSP++ installation directory. Please refer to the readme file provided with each example for more information.

Background Telemetry Channel

Some USB debug agents support the Background Telemetry Channel (BTC), which facilitates data exchange between VisualDSP++ and the processor without interrupting processor execution.

This revision of the ADSP-21364 EZ-KIT Lite does not support the Background Telemetry.

VisualDSP++ Interface

This section provides information about the following parts of the VisualDSP++ graphical user interface:

- "Boot Load" on page 1-11
- "Target Options" on page 1-12
- "Core Hang Conditions" on page 1-13
- "Hardware Breakpoints" on page 1-15

Boot Load

Choosing **Boot Load** from the **Settings** menu runs the processor and performs a hard reset on the board. This command saves you from having to shut down VisualDSP++, reset the EZ-KIT Lite board, and bring up VisualDSP++ again when you want to perform a hard reset.

Use this feature when loading debug boot code from an external part or when you want to put the device into a known state.

Target Options

Choosing **Target Options** from the **Settings** menu opens the **Target Options** dialog box (Figure 1-2). Use target options to control certain aspects of the processor on the ADSP-21364 EZ-KIT Lite evaluation system.

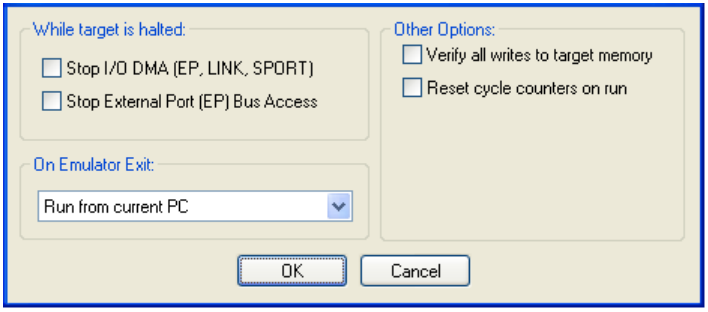

Figure 1-2. Target Options Dialog Box

While Target is Halted and On Emulator Exit Options

This target option controls the processor's behavior when VisualDSP++ relinquishes processor control (for example, when exiting VisualDSP++). The options are detailed in Table 1-4 and Table 1-5.

Other Options

Table 1-6 describes other available target options.

Table 1-4. While Target is Halted Options

Option	Description
Stop I/O DMA	Stops IO DMAs in emulator space. This option disables DMA requests when the emulator has control of the processor. data in the **EP**, **LINK**, or **SPORT DMA** buffers are held there unless the internal **DMA** request was already granted. This option holds off incoming data and ceases outgoing data. Because SPORT-receive data cannot be held off, it is lost, and the overrun bit is set. The direct write buffer (internal memory write) and the EP pad buffer are allowed to flush any remaining data to internal memory.
Stop External Port (EP) Bus Access	Stops IO processor external port (EP) operation in emulator space. This option disables all EP requests when the emulator has control of the processor. After acknowledging an emulation interrupt, this option deasserts ACK (deasserts REDY if host access), preventing further data from being accepted if the EP is accessed.

Table 1-5. On Emulator Exit Options

Option	Description
On Emulator Exit	Determines the state the processor is left in when the emulator relinquishes control of the processor: **Reset DSP and Run** causes the processor to reset and begin execution from its reset vector location. **Run from current PC** causes the processor to begin running from its current location.

Core Hang Conditions

Certain peripheral devices, such as host ports, DMA, and link ports, can hold off the execution of processor instructions. This is known as a hung condition and commonly occurs when reading from an empty port or writing to a full port. If an attempt to halt the processor is made during one of these conditions, the EZ-KIT Lite may encounter a core hang.

Normally, a core hang can be cleared by the board using a special clear/abort bit. However, there are cases in which it is desirable or possible not to clear the core hang. Sometimes it is desirable to wait for the core

Table 1-6. Other Target Options

Option	Description
Verify all writes to target memory	Validates all memory writes to the processor. After each write, a read is performed and the values are checked for a matching condition. Enable this option during initial program development to locate and fix initial build problems (such as attempting to load data into non-existent memory). Clear this option to increase performance while loading executable files since VisualDSP++ does not perform the extra reads that are required to verify each write.
Reset cycle counters on run	Resets the cycle count registers to zero before a **Run** command is issued. Select this option to count the number of cycles executed between breakpoints in a program.

hang to clear itself, such as when waiting for a host processor to read or write data. In other cases, it is not possible to clear the core hang, and a processor reset must occur to continue the debugging session.

Table 1-7 describes the EZ-KIT Lite's core hang operations.

Table 1-7. Core Hang Operations

Option	Description
Abort	Abort the hung operation. This causes the offending instruction to be aborted in the pipeline.
Retry	Allows you to remedy the hung operation. For example, if a host processor is holding off the processor, you can cause the host to clear the hung condition.
Ignore	Performs a software reset on the target board.
Clear	Aborts the hung operation. This causes the offending instruction to be aborted in the pipeline.
Acknowledge	Allows you to remedy the hung operation. For example, if a host processor is holding off the processor, you can cause the host to clear the hung condition.
Reset	Performs a software reset on the target board.

Hardware Breakpoints

Hardware breakpoints work similarly to watchpoints. Set hardware breakpoints on:

- Data transfers within a user-defined memory range
- Instructions
- Register reads and writes

To enable hardware breakpoints for ADSP-21364 processors:

1. From the **Settings** menu, choose **Hardware Breakpoints**.
2. The **Hardware Breakpoints** dialog box appears. The dialog box has three tabbed pages: **Data**, **Instruction**, and **Other** (Figure 1-3).

Figure 1-3. Hardware Breakpoints Dialog Box

Refer to the following sections for information about breakpoint types.

- "Data Hardware Breakpoints" on page 1-16
- "Instruction Hardware Breakpoints" on page 1-17
- "Other Breakpoints" on page 1-18

Regardless of the breakpoint type, all of the breakpoints share the attributes and option settings described in:

- "Common Hardware Breakpoint Attributes" on page 1-19
- "Global Hardware Breakpoint Options" on page 1-19

Additional information about hardware breakpoints can be found in "Miscellaneous" on page 1-19.

Data Hardware Breakpoints

For ADSP-21364 processors, use data breakpoints to break on accesses to internal memory and IOP registers.

An action, such as `DAG1` or `DM()` modifier access, triggers a data breakpoint. The two data breakpoints are ORed to generate a single data breakpoint condition.

The **Data** page of the **Hardware Breakpoints** dialog box, which permits the specification of the data breakpoints, is shown in Figure 1-4.

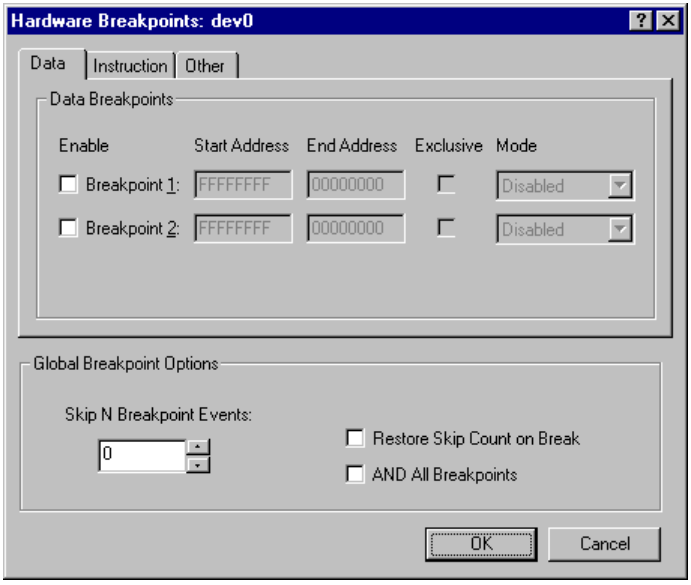

Figure 1-4. Data Page of Hardware Breakpoints Dialog Box

Instruction Hardware Breakpoints

For ADSP-21364 processors, an instruction breakpoint occurs when an instruction is executed within one of the specified address ranges. The four individual instruction breakpoints are ORed to generate a single instruction breakpoint condition.

Shown in Figure 1-5 is the **Instruction** page of the **Hardware Breakpoints** dialog box, which permits the specification of four individual instruction breakpoints.

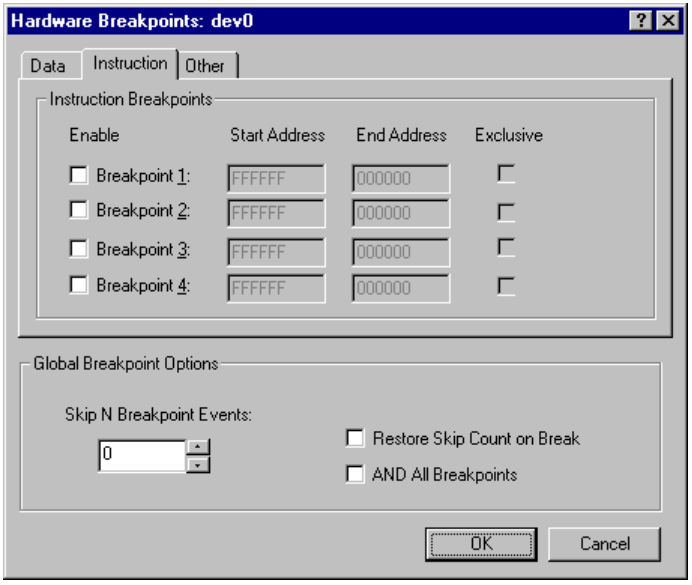

Figure 1-5. Instruction Page of Hardware Breakpoints Dialog Box

Other Breakpoints

For the ADSP-21364 SHARC processor, the **Other** page of the **Data Breakpoints** dialog box (Figure 1-6) permits the specification of hardware breakpoints triggered by access to PM data and IO.

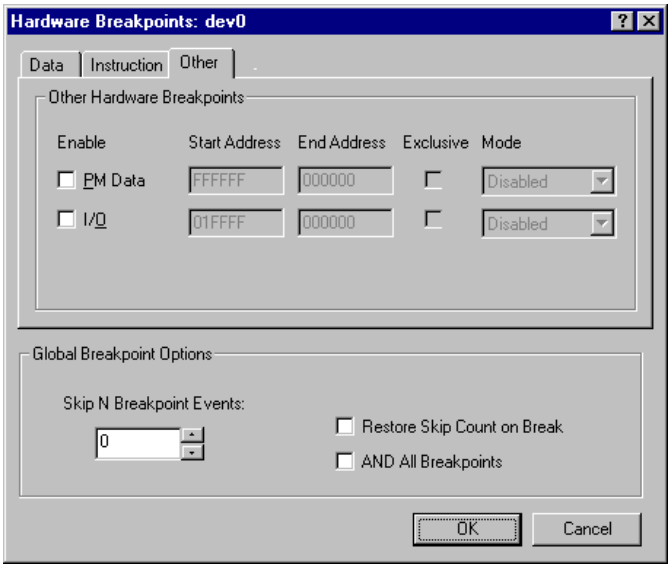

Figure 1-6. Other Page of Hardware Breakpoints Dialog Box

Table 1-8. Other Hardware Breakpoint Options

Option	Description
PM DataEvents	Enables PM data breakpoints.PM data breakpoints are similar to data breakpoints (Data page), except accesses that trigger a PM breakpoint are made by DAG2 or the PM() modifier. Like data breakpoints, PM data breakpoints cause a break on accesses to internal memory, IOP registers, the external port (EP), and multiprocessor memory space (MMS).
I/O	Enables IO breakpoints.IO breakpoints are triggered by accesses made on the IO Address Bus. Use an IO breakpoint to break on accesses made during DMA transfers, MMS accesses, and Host accesses.

Common Hardware Breakpoint Attributes

Each of the three tabs in the **Hardware Breakpoints** dialog box has common attributes described in Table 1-9.

Table 1-9. Common Hardware Breakpoint Attributes

Attribute	Description
Enable	Enables each individual breakpoint.
Start Address **End Address**	Specify inclusive start and end addresses. Each pair of addresses sets up an address range for the particular breakpoint.
Exclusive	Enables breaks outside of the specified (inclusive) address range.
Mode	**Data** page and **Other** page only. This option specifies the modes that trigger hardware breakpoints. The available choices are: **Disabled**—disables the breakpoint **On Write**—triggers the breakpoint on any write operation to the specified address range **On Read**—triggers the breakpoint on any read operation from the specified address range **Any Access**—triggers the breakpoint on any read or write access to the specified address range.

Global Hardware Breakpoint Options

For ADSP-21364 processors, the options listed in Table 1-10 apply to all hardware breakpoints, regardless of their type.

Miscellaneous

Be aware of the following tips and tricks when using hardware breakpoints on ADSP-21364 processors (see Table 1-11).

Table 1-10. Global Hardware Breakpoint Options

Option	Description
Skip N Breakpoint Events	Sets the Skip Count—specifies the number of breakpoint events to be ignored before stopping the processor. Each time a hardware breakpoint condition occurs, the count decrements. When the count reaches zero (0), the processor processes the hardware break. Use this option to count the number of times a break operation occurs. Breakpoints within the group are ORed together to create this condition.
Restore Skip Count on Break	When checked, causes the emulator to restore the Skip Count to the value at program restart. Otherwise, the Skip Count remains at its current value.
AND All Breakpoints	ANDs the interrupts to form the composite interrupt. Normally, the group interrupts are ORed to create a composite interrupt.

Table 1-11. Hardware Breakpoint Restrictions

Category	Description
Latency	For SHARC processors, hardware breakpoints do not assert until two (2) instruction cycles after the actual break condition occurs.
Placement	• Do not place hardware breaks at any address where a JUMP, CALL, or IDLE instruction is illegal. • Do not place breaks in the last few instructions of a DO LOOP or in the delay slots of a delayed branch. For more information on these illegal locations, refer to the Hardware Reference manual for the target processor. • To set a breakpoint on a single address, set the **Start Address** equal to the **End Address**.

2 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-21364 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the ADSP-21364 board and explains how the board components interface with the processor.
- "Switch Settings" on page 2-8
  Shows the location and describes the function of the board switches.
- "LEDs and Push Buttons" on page 2-12
  Shows the location and describes the function of the board LEDs and push buttons.
- "Connectors" on page 2-15
  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

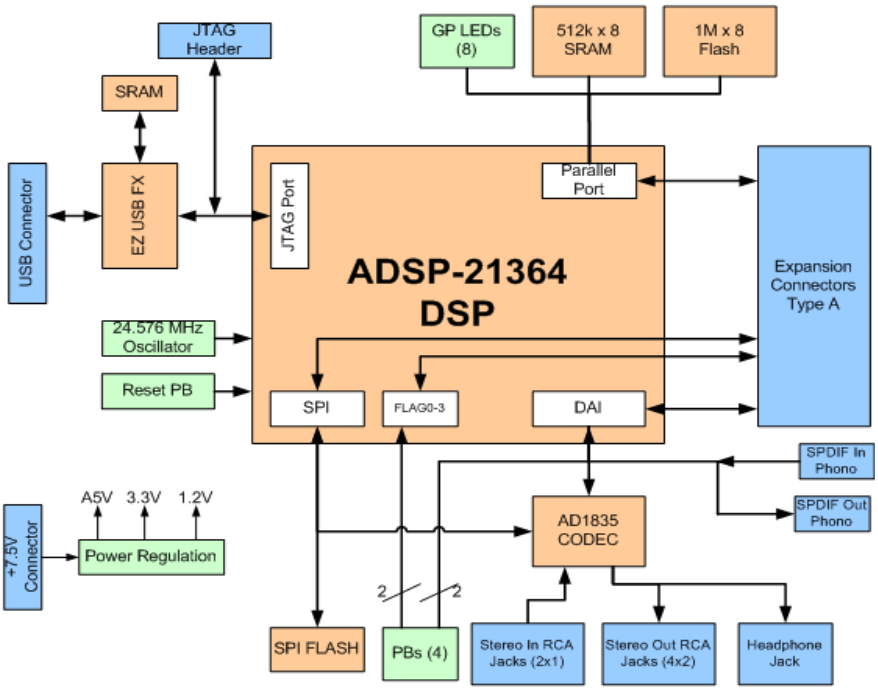

Figure 2-1. System Architecture Block Diagram

The EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-21364 processor. The processor core is powered at 1.2V, and the IO is powered at 3.3V. Two 0-ohm resistors give access to the processor's power planes and allow to measure the power consumption of the processor. The `R79` resistor provides access to the IO voltage of the processor, and the `R80` resistor provides access to the core voltage plane of the processor.

The CLKIN pin of the processor connects to a 24.576 MHz oscillator. The core frequency of the processor is derived by multiplying the frequency at the CLKIN pin by a value determined by the state of the processor pins, CLKCFG1 and CLKCFG0. The value at these pins is determined by the state of the SW10 switch (see "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11). By default, the EZ-KIT Lite gives a core frequency of 147.456 MHz. It is possible to increase the speed of the processor by changing the value of the PMCTL register.

The SW10 switch also configures the boot mode of the processor. The EZ-KIT Lite is capable of Parallel Port boot and SPI Master Boot. By default, the EZ-KIT Lite boots from the parallel port. For information about configuring the boot modes, see "Boot Mode and Clock Ratio Select Switch (SW10)" on page 2-11.

Parallel Port

The parallel port (PP) of the ADSP-21364 processor consists of a 16-bit multiplex address/data memory bus (AD15-0) and an address latch-enable pin (ALE). The interface does not have any memory select pins; these signals must be generated by decoding the address.

The PP connections to the EZ-KIT Lite are shown in Figure 2-2. The PP is connected to an 8-bit parallel flash memory, an 8-bit SRAM memory, and eight general-purpose LEDs. The upper three address bits are connected to a 3-to-8 decoder, providing eight memory select pins. See "External Memory" on page 1-6 for more information about accessing the flash and SDRAM memories.

Because the PP is a multiplexed address/data memory bus, two 8-bit latches are used to latch the upper address bits. Additional latch is used to drive the LEDs. The latter allows the LED values to be written to as if they were at a memory location. For more information about using the LEDs, refer to the "LEDs and Push Buttons" on page 1-9.

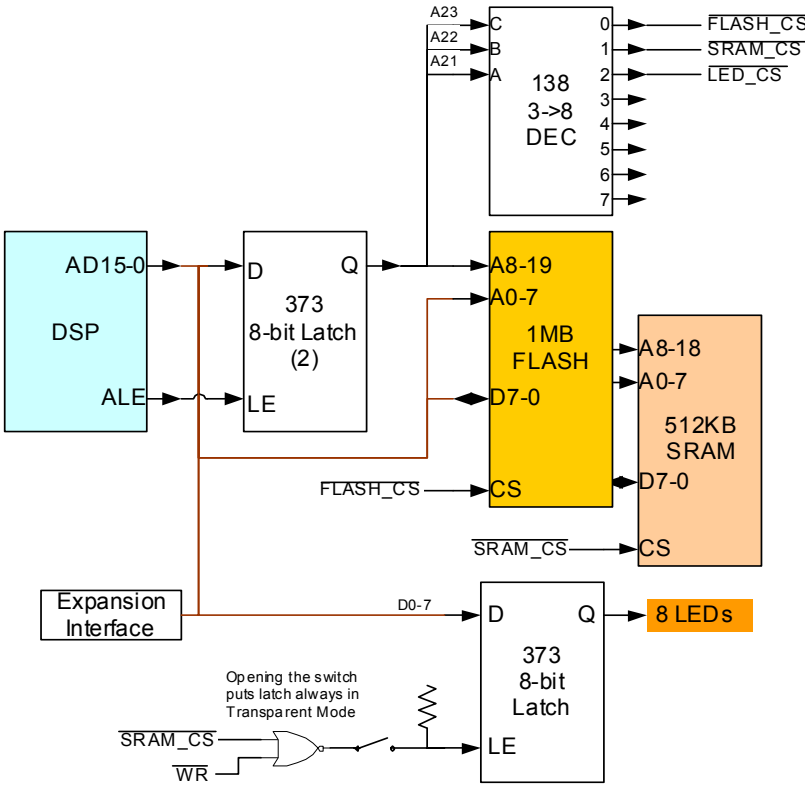

Figure 2-2. Parallel Port Connections Block Diagram

All of the PP signals are available externally via the expansion interface connectors (J3-1). The pinout of the connectors can be found in "Schematics" on page B-1.

DAI Interface

The pins of the Digital Application Interface (DAI) connect to the signal routing unit (SRU). The SRU is a flexible routing system, providing a large system of signal flows within the processor. In general, the SRU allows to route the DAI pins to different internal peripherals in various combinations.

The DAI pins are connected to the AD1835A audio codec, a 26-pin header, 2 RCA connectors, the audio oscillator output, and two push buttons. Figure 2-3 illustrates the EZ-KIT Lite's connections to the DAI.

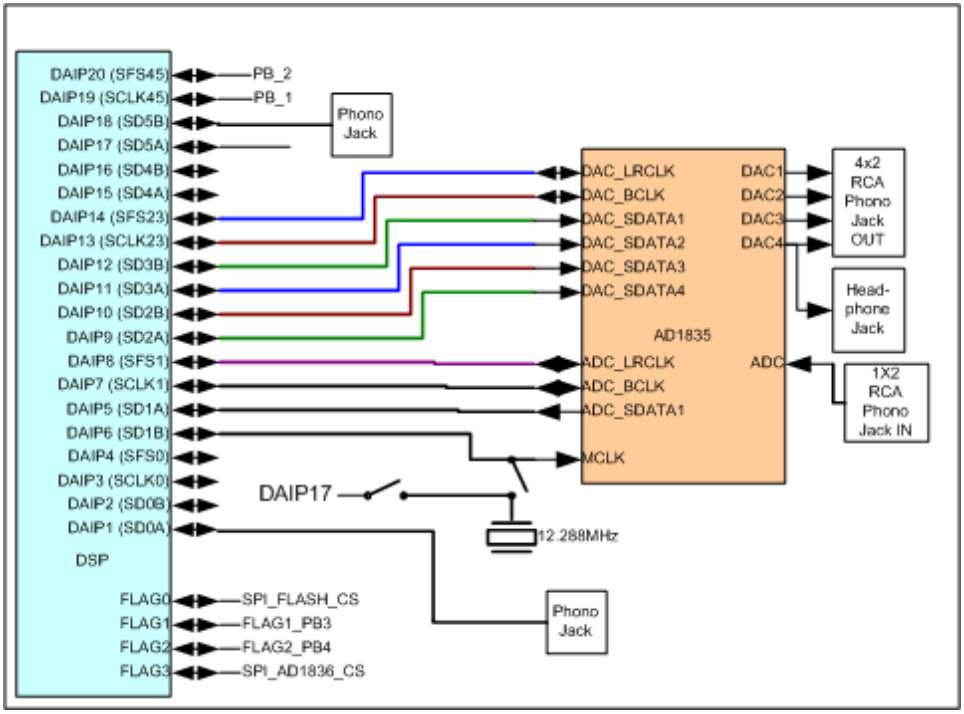

Figure 2-3. DAI Connections Block Diagram

To use the DAI for a different purpose, disable any signal driving the DAI pins, with a switch. See "Codec Setup Switch (SW7)" on page 2-8 for how to. In addition, the codec setup switch allows flexible routing of the 12.288 MHz audio oscillator's output signal. By default, this signal is used as the master clock (MCLK) for the AD1835A codec.

All of the DAI signals are available externally via the expansion interface connectors (J3-1), as well as the 0.1' spaced header P3. The pinout of these connectors can be found in "Schematics" on page B-1.

SPI Interface

The serial peripheral interconnect (SPI) interface of the processor connects to an SPI flash memory and the AD1835A audio codec. The FLAG0 pin is used as a memory select for accessing the SPI flash memory, and the FLAG3 pin is used for accessing the AD1835A's configuration registers.

All of the SPI signals are available externally via the expansion interface connectors (J3-1), as well as the 0.1' spaced header P2. The pinout of these connectors can be found in "Schematics" on page B-1.

FLAG Pins

The processor has four general-purpose IO FLAG pins. Table 2-1 describes the connection of each flag.

Table 2-1. IO FLAG Pins

FLAG Pin	EZ-KIT Lite Function
FLAG0	SPI flash chip select
FLAG1	Push button (SW1) input
FLAG2	Push button (SW2) input
FLAG3	AD1835A SPI interface chip select

For information on how to disable the push buttons from driving the corresponding processor flag pin, see section "Push Button Enable Switch (SW9)" on page 2-10.

The FLAG signals are available externally via the expansion interface connectors (J3-1). The pinout of these connectors can be found in "Schematics" on page B-1.

Expansion Interface

The expansion interface consists of the three 90-pin connectors. Table 2-2 shows the interfaces each connector provides. For the exact pinout of these connectors, refer to Appendix B, "Schematics" on page B-1. The mechanical dimensions of the connectors can be obtained from Technical or Customer Support.

Table 2-2. Expansion Interface Connectors

Connector	Interfaces
J1	5V, AD15-0
J2	3.3V, FLAG3-0, DAI_P20-1, SPI
J3	5V, 3.3V, Reset, Parallel Port Control signals

Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the internal and external memory of the processor through a 6-pin interface. The JTAG emulation port of the processor is also connected to the USB debugging interface. When an emulator connects to the board at P5, the USB debugging interface is disabled. This is not the standard connection of the JTAG interface.

For information about the standard connection of the interface, see *EE-68* published on the Analog Devices Web site. For more information about the JTAG connector, see "JTAG Header (P5)" on page 2-19. To learn more about available emulators, contact Analog Devices (see "Product Information").

Switch Settings

Figure 2-4 shows the location and default settings of the EZ-KIT Lite switches.

Electret Microphone Select Switch (SW6)

To connect an electret microphone to the audio input, place all positions of the SW6 switch "ON". The default position of this switch is all "OFF". When all of the switches are in the "ON" position, a DC offset of 2.5V is added to the signal, and gain of the input amplifiers is changed from 1x to 10x.

Codec Setup Switch (SW7)

The codec setup switch (SW7) can be used to change the routing of some of the signals going to the AD1835A codec and to setup the communication protocol of the codec.

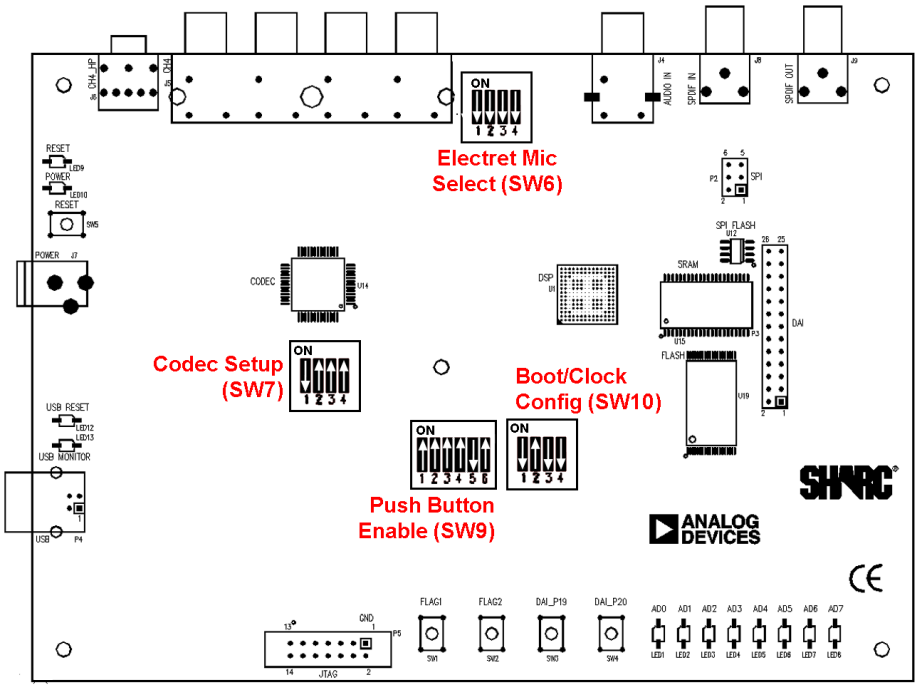

Figure 2-4. DIP Switch Locations and Default Settings

Positions 1 and 2 determine the clock routing for the audio oscillator to the codec and to the processor. Figure 2-5 illustrates how the switch positions 1 and 2 are connected on the board. In the default position, route the DAI_P17 pin to DAI_P6 (in software) to clock the AD1835A.

Position 3 of the SW7 switch determines if the AD1835A device is a master or is a slave. If the AD1835A is a master, the device's serial interface generates the frame sync and clock signals necessary to transfer data. When the device is a slave, the processor must generate the frame sync and clock signals. By default, position 3 is "ON", and the AD1835A generates the control signals.

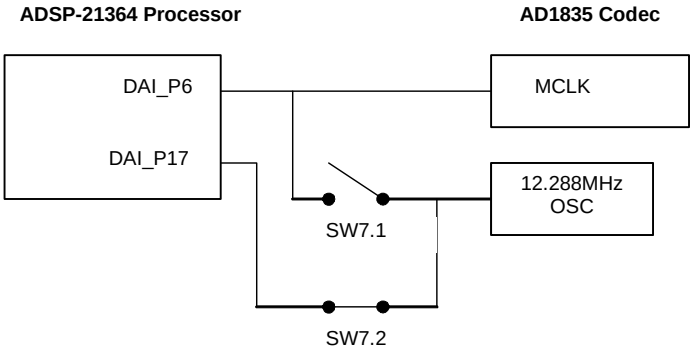

Figure 2-5. Audio Clock Routing

Position 4 of SW7 disconnects the AD1835A's ADC_DATA pin from the DAI interface. This is useful when the DAI interface connects to another device.

Push Button Enable Switch (SW9)

The push button enable switch (SW9) disconnects the push buttons from the corresponding processor pins. This allows the signals to be used for another purpose. Table 2-3 shows the signal and SW9 connections. By default, all of the position of the SW9 switch are "ON", allowing the push buttons to function as designed.

Table 2-3. Push Button Enable Switch (SW9) Connections

Switch Position	Push Button Reference Designator	Processor Pin
1	SW1	FLAG1
2	SW2	FLAG2
3	SW3	DAI19
4	SW4	DAI20

Position 6 of SW9 connects or disconnects the latch-enable pin of the LED to the logical "OR" of the ~WE and ~LED_CS signals. When position is "OFF", the latch-enable pin of the LED latch ((U24) is always pulled "HIGH", making the latch transparent. In this position, the value of the LEDs is directly connected to AD7-0. When position 6 is "ON", the values of the LEDs are set by writing to a memory location. The lower 8 bits of the data written to the address 0x1400 0000 set the values of the LEDs. By default, position 6 is "ON", allowing the LEDs to be written by writing to a memory address. For more information refer to "LEDs and Push Buttons" on page 1-9.

Boot Mode and Clock Ratio Select Switch (SW10)

The SW10 switch sets the boot mode and clock multiplier ration. Table 2-4 shows how to set up the boot mode using positions 1 and 2. By default, the EZ-KIT Lite boots in Parallel Port mode from flash memory.

Table 2-4. Boot Mode Configuration

BOOTCFG1 Pin (Position 2)	BOOTCFG0 Pin (Position 1)	Boot Mode
OFF	OFF	SPI Slave Boot
OFF	ON	SPI Master Boot
ON	**OFF**	**Flash Boot**[1]
ON	ON	Internal Boot Mode

1 Bold typeface denotes the default setting.

Table 2-5 shows how to set up the clock multiply ratio using positions 3 and 4. By default, the processor increases the clock multiply ratio by six, setting the core clock to 147.456 MHz.

Table 2-5. Core Clock Rate Configuration

CLKCFG1 (Position 4)	CLKCFG0 (Position 3)	Core to CLKIN Ratio
OFF	OFF	6:1
OFF	ON	32:1
ON	**OFF**	**16:1**[1]
ON	ON	NA

1 Bold typeface denotes the default ratio.

Loop-Back Test Switch (SW11)

The loop-back test switch (SW11) is located at the bottom of the board. This switch is used only for testing; all switch positions should be OFF.

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 2-6 shows the locations of the LEDs and push buttons.

General Purpose LEDs (LED8–1)

Eight general-purpose LEDs are connected to the processor through a latch on signals AD7-0. These LEDs can be accessed by writing to the FLAG registers or by writing to a memory address. Refer to "LEDs and Push Buttons" on page 1-9 for more information.

Reset LEDs (LED9 and LED12)

When LED9 is lit (red), the master reset of all the major ICs is active. When LED12 is lit (red), the USB interface chip (U34) is being reset. The USB chip is reset only on power-up, or if USB communication has not been initialized.

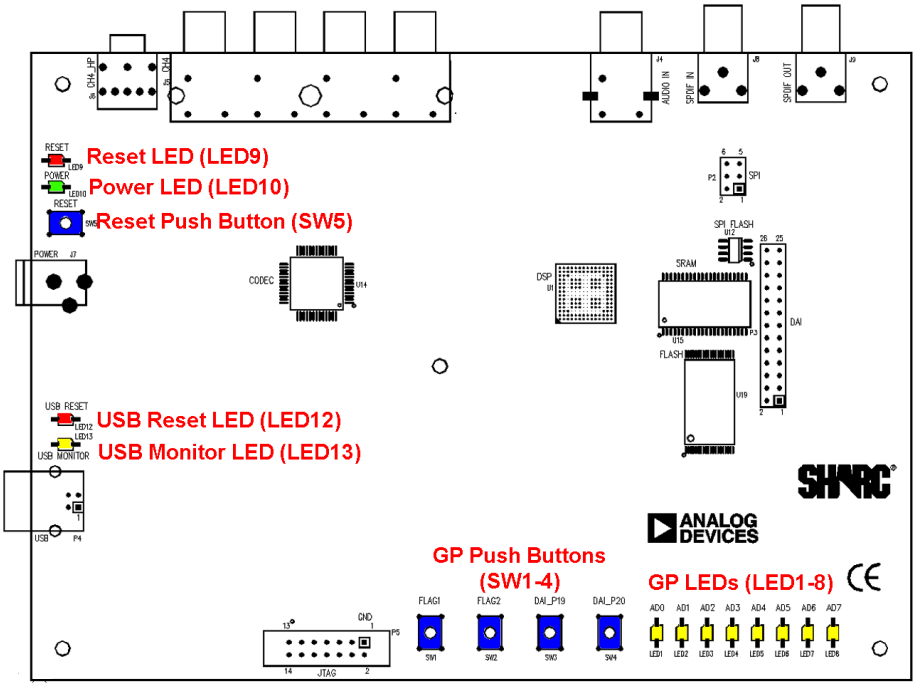

Figure 2-6. LED and Push Button Locations

Power LED (LED10)

When LED10 is lit (green), it indicates that power is being properly supplied to the board.

USB Monitor LED (LED13)

The USB monitor LED (LED13) indicates that USB communication has been initialized successfully and you may connect to the processor using a VisualDSP++ EZ-KIT Lite session. Once the USB cable is plugged into the board, it takes approximately 15 seconds for the USM monitor LED

to light. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver (see the *VisualDSP++ Installation Quick Reference Card*).

When VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Push Buttons (SW4–1)

Four push buttons (SW4-1) are provided for general-purpose user input. Two of the push buttons are connected to the FLAG pins of the processor. The other two are connected to the DAI of the processor. The push buttons are active "HIGH" and, when pressed, send a High (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-9 for more information. The push button enable switch (SW9) is capable of disconnecting the push buttons from the corresponding processor pin (refer to "Push Button Enable Switch (SW9)" on page 2-10 on page 3-10 for more information). The processor signals and corresponding push buttons are summarized in Table 2-6.

Table 2-6. Push Button Connections

Processor Signal	Push Button Reference Designator	Processor Signal	Push Button Reference Designator
FLAG1	SW1	DAI_P19	SW3
FLAG2	SW2	DAI_P20	SW4

Board Reset Push Button (SW5)

The RESET push button (SW5) resets all of the ICs on the board. The only exception is the USB interface chip (U34). The chip is not being reset when the push button is pressed after the USB cable has been plugged in

and communication correctly initialized with the PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.

Connectors

This section describes the connector functionality and provides information about mating connectors. Figure 2-7 shows the connector locations.

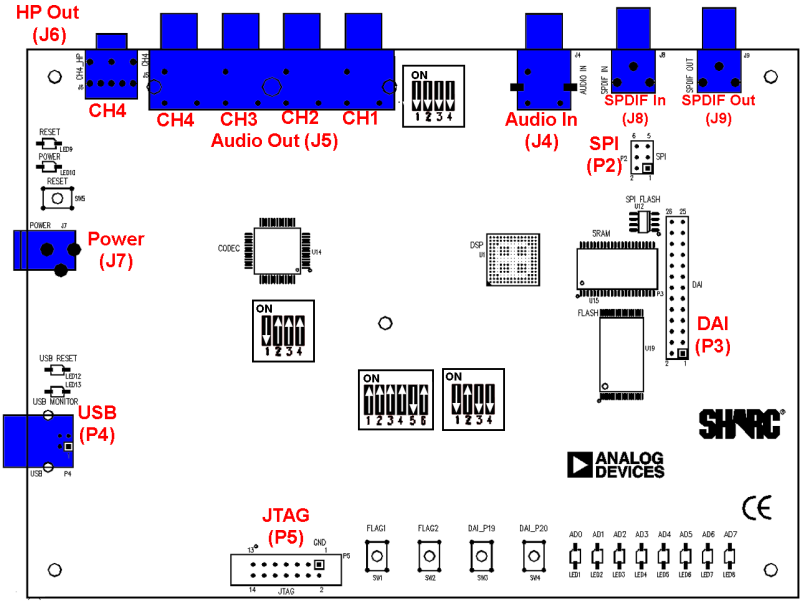

Figure 2-7. Connector Locations

Expansion Interface (J3–J1)

Three board-to-board connectors (J3-1) provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see "Expansion Interface" on page 2-7. For the J3-1 connectors' availability and pricing, contact Samtec.

Part Description	Manufacturer	Part Number
90 Position 0.05" Spacing, SMT (J1, J2, J3)	Samtec	SFC-145-T2-F-D-A
Mating Connector		
90 Position 0.05" Spacing (Through Hole)	Samtec	TFM-145-x1 Series
90 Position 0.05" Spacing (Surface Mount)	Samtec	TFM-145-x2 Series
90 Position 0.05" Spacing (Low Cost)	Samtec	TFC-145 Series

Audio In RCA Connector (J4)

Part Description	Manufacturer	Part Number
Two channel right angle RCA jack	Switchcraft	PJRAS1X2S02
Mating Cable		
Two channel RCA interconnect cable	Monster Cable	BI100-1M

Audio Out RCA Connector (J5)

Part Description	Manufacturer	Part Number
Six channel right angle RCA jack	Switchcraft	PJRAS2X2S01
Mating Cable		
Two channel RCA interconnect cable	Monster Cable	BI100-1M

Headphone Out Jack (J6)

Part Description	Manufacturer	Part Number
3.5mm stereo jack (J6)	Shogyo	SJ-0359AM-5

Power Jack (J7)

The power connector (J7) provides all of the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm Power Jack (J7)	Switchcraft Digi-Key	RAPC712 SC1152-ND
Mating Power Supply (shipped with EZ-KIT Lite)		
7.5V Power Supply	GlobTek	TR9CC2000LCP-Y

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-7 shows the power supply specifications.

Table 2-7. Power Supply Specifications

Terminal	Connection
Center pin	+7.5 VDC@2A
Outer Ring	GND

SPDIF Coax Connectors (J8 and J9)

Part Description	Manufacturer	Part Number
Coaxial (J8, J9)	Switchcraft	PJRAN1X1U01
Mating Cable		
Two channel RCA interconnect cable	Monster Cable	BI100-1M

SPI Header (P2)

The SPI connector (P2) provides access to all of the SPI signals in the from of a .1" spacing header. In addition, the FLAG1 signal can be used as a chip select. If you are using FLAG1 as a chip select, disable the push button associated with the flag. For more information, see "Push Button Enable Switch (SW9)" on page 2-10.

Part Description	Manufacturer	Part Number
6-pin IDC Header (P2)	Sullins	PTC04DAAN

DAI Header (P3)

The DAI connector (P3) provides access to all of the DAI signals in the from of a .1" spacing header. When using the header to access the DAI pins of the processor, ensure that signals, which normally drive the DAI pins, are disabled. Refer to "Codec Setup Switch (SW7)" on page 2-8 for more information on how to disable signals already being driven from elsewhere on the EZ-KIT Lite.

Part Description	Manufacturer	Part Number
26-pin IDC Header (P3)	Berg	54102-T08-13

USB Connector (P4)

The USB connector (P4) allows to configure and program the processor.

Part Description	Manufacturer	Part Number
Type B USB receptacle (P4)	Mill-Max Digi-Key	897-30-004-90-000 ED90003-ND

JTAG Header (P5)

The JTAG header (P5) is the connecting point for a JTAG in-circuit emulator pod. When an emulator is connected to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

Part Description	Manufacturer	Part Number
14-pin IDC Header (P5)	Berg	54102-T08-07

A BILL OF MATERIALS

The bill of materials corresponds to the board schematics on page B-1. Please check the latest schematics on the Analog Devices website, http://www.analog.com/Processors/Processors/DevelopmentTools/technicalLibrary/manuals/DevToolsIndex.html#Evaluation%20Kit%20Manuals.

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
1	1	AM29LV08IB-120EC TSOP40 1M-X-8-FLASH-3V	U19	AMD	AM29LV081-120EC
2	2	74LVC14A SOIC14 HEX-INVER-SCHMITT-TRIG-GER	U28, U33	TI	74LVC14AD
3	1	CY7C64603-128 PQFP128 USB-TX/RX MICROCONTROL-LER	U34	CYPRESS	CY7C64603-128NC
4	1	MMBT4401 SOT-23 NPN TRANSISTOR 200MA	Q1	FAIRCHILD	MMBT4401
5	1	24.576MHZ 1/2 OSC001 OSC	U16	EPSON	SG-531P 24.576MC2
6	1	CY7C1019BV33-15VC SOJ32	U29	CYPRESS	CY7C1019BV33-12VC
7	1	AD8532AR SOIC8 DUAL AMP 250MA	U10	ANALOG DEVICES	AD8532AR
8	2	SN74AHC1G02 SOT23-5 SINGLE-2 INPUT-NOR	U26, U36	TI	SN74AHC1G02DBVR
9	1	SN74LV164A SOIC14 8-BIT-PARALLEL-SERIAL	U35	TI	SN74LV164AD
10	1	CY7C4201V-15AC TQFP32 64-BYTE-FIFO	U32	CYPRESS	CY7C4201V-15AC
11	1	12.0MHZ THR OSC006 CRYSTAL	Y1	DIG01	300-6027-ND
12	2	SN74AHC1G00 SOT23-5 SINGLE-2-INPUT-NAND	U20, U27	TI	SN74AHC1G00DBVR

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
13	1	12.288MHZ SMT OSC003 TS201/21262	U17	DIG01	SG-8002CA-PCC-ND
14	1	74LVC138AD SOIC16 3-TO-8-DEMUX	U25	PHILIPS	74LVC138AD
15	3	74LVC373APW TSSOP20 8-BIT-D-LATCH	U18, U21, U24	PHILIPS	74LVC373APW
16	1	IS61LV5128AL TSOP44 512KX8-SRAM	U15	ISSI	IS61LV5128AL-10T
17	1	AT25F512N SOIC8 SPI-FLASH-512KB	U12	ATMEL	AT25F512N-10SI-2.7
18	1	LTC1877 MSOP8 600MA ADJ SWITCHING REG	VR5	LINEAR TECH	LTC1877EMS8
19	1	74LVCU04AD SOIC14 UNBUF-FERED-HEX-INVERTER	U3	DIGI-KEY	296-9861-1-ND
20	1	21364 24LC00 “U23” see 1000127	U23	MICROCHIP	24LC32A-I/SN
21	2	1000pF 50V 5% 1206 CERM	C37-38	AVX	12065A102JAT2A
22	8	2200pF 50V 5% 1206 NPO	C67-74	AVX	12065A222JAT050
23	1	ADM708SAR SOIC8 VOLTAGE-SUPERVISOR	U22	ANALOG DEVICES	ADM708SAR
24	1	ADP3339AKC-33 SOT-223 3.3V 1.5A REGULATOR	VR2	ANALOG DEVICES	ADP3339AKC-3.3-RL

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
25	2	ADP3336ARM MSOP8 ADJ 500MA REGULATOR	VR1, VR4	ANALOG DEVICES	ADP3336ARM-REEL
26	8	AD8606AR SOIC8 OPAMP	U2, U4-9, U11	ANALOG DEVICES	AD8606AR
27	1	AD1835AAS MQFP52 2IN-8OUT-96KHZ-CODEC	U14	ANALOG DEVICES	AD1835AAS
28	1	ADSP-21364 BGA136 SHARC-EX-DSP	U1	ANALOG DEVICES	ADSP-21364SKBC-ENG
29	5	RUBBER FEET BLACK	MH1-5	MOUSER	517-SJ-5018BK
30	1	PWR 2.5MM_JACK CON005 RA	J7	SWITCH-CRAFT	SC1152-ND12
31	1	USB 4PIN CON009 USB	P4	MILL-MAX	897-30-004-90-000000
32	1	RCA 4X2 CON011 RA	J5	SWITCH-CRAFT	PJRAS4X2U01
33	2	RCA 1X1 CON012 BLK	J8-9	SWITCH-CRAFT	PJRAN1X1U01
34	5	SPST-MOMENTARY SWT013 6MM	SW1-5	PANASONIC	EVQ-PAD04M
35	3	0.05 45X2 CON019 SMT SOCKET	J1-3	SAMTEC	SFC-145-T2-F-D-A
36	1	DIP8 SWT016	SW11	C&K	TDA08H0SK1
37	1	DIP6 SWT017	SW9	C&K	TDA06H0SK1

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
38	3	DIP4 SWT018 4PIN-SMT-SWT	SW6-7, SW10	DIG01	CKN1363-ND
39	1	RCA RCA_1X2 CON031 RA	J4	SWITCH- CRAFT	PJRAS1X2S02
40	2	0.00 1/8W 5% 1206	R82, R91	YAGEO	0.0ECT-ND
41	9	AMBER-SMT LED001 GULL-WING	LED1-8, LED13	PANASONIC	LN1461C-TR
42	8	330pF 50V 5% 805 NPO	C104, C106, C108, C110, C112, C114, C116, C118	AVX	08055A331JAT
43	15	0.01uF 100V 10% 805 CERM	C1, C22, C127, C153, C155, C157-164, C166, C182	AVX	08051C103KAT2A
44	8	0.22uF 25V 10% 805 CERM	C77, C87, C99-102, C111, C131	AVX	08053C224FAT
45	28	0.1uF 50V 10% 805 CERM	C21, C47, C57, C59, C120-121, C132-133, C141, C148, C152, C156, C165, C167-181	AVX	08055C104KAT
46	4	0.001uF 50V 5% 805 NPO	C82-83, C88, C98	AVX	08055A102JAT2A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
47	39	10K 100MW 5% 805	R17, R64, R66, R70-71, R74, R76-78, R90, R92, R96-102, R107-108, R110-111, R152, R159-167, R169-175	PHYCOMP	9C08052A1002JLHFT
48	3	33 100MW 5% 805	R68, R81, R109	AVX	CR21-330JTR
49	3	4.7K 100MW 5% 805	R72, R95, R176	AVX	CR21-4701F-T
50	1	1M 100MW 5% 805	R168	AVX	CR21-1004F-T
51	2	1.5K 100MW 5% 805	R105, R189	AVX	CR21-1501F-T
52	2	2.00K 1/8W 1% 1206	R3, R5	DALE	CR32-2001F-T
53	10	49.9K 1/8W 1% 1206	R114-115, R117-124	AVX	CR32-4992F-T
54	2	2.21K 1/8W 1% 1206	R93-94	AVX	CR32-2211F-T
55	12	100pF 100V 5% 1206 NPO	C2-12, C64	AVX	12061A101JAT2A
56	2	10uF 16V 10% B TANT	CT13-14	AVX	TAJB106K016R
57	4	100 100MW 5% 805	R185-188	AVX	CR21-101J-T
58	2	301 1/4W 1% 1206	R1-2	BOURNS	CR1206-FX-3010
59	9	220pf 50V 10% 1206 NPO	C90-97, C183	AVX	12061A221JAT2A
60	2	2A S2A_RECT DO-214AA SILICON RECTIFIER	D1-2	GENER-ALSEMI	S2A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
61	6	600 100MHZ 500MA 1206	FER2, FER4-8	DIGIKEY	240-1019-1-ND
62	1	100 1/8W 5% 1206	R8	PANASONIC	ERJ-8GEYJ101V
63	4	237 1/8W 1% 1206	R13-14, R18, R20	AVX	CR32-2370F-T
64	2	750K 1/8W 1% 1206	R11, R116	DALE/VISHAY	CRCW12067503FRT1
65	4	5.76K 1/8W 1% 1206	R6, R10, R19, R22	PHYCOMP	9C12063A5761FKHFT
66	10	11.0K 1/8W 1% 1206	R47, R49-50, R52-53, R55-56, R58, R113, R136	DALE	CRCW12061102FRT1
67	6	1uF 16V 10% 805 X7R	C39, C44, C48, C56, C58, C61	MURATA	GRM40X7R105K016AL
68	1	75 1/8W 5% 1206	R4	PHILIPS	9C12063A75R0JLHFT
69	3	30pF 100V 5% 1206	C55, C62-63	AVX	12061A300JAT2A
70	1	10 100MW 5% 805	R150	DALE	CRCW0805-10R0FRT1
71	1	249K 1/10W 1% 805	R86	DALE	CRCW0805-2493FRT1
72	1	124K 1/10W 1% 805	R83	DALE	CRCW0805-1243FT
73	12	680pF 50V 1% 805 NPO	C76, C80-81, C89, C103, C105, C107, C109, C113, C115, C117, C119	AVX	08055A681FAT2A
74	3	10uF 25V +80-20% 1210 Y5V	C46, C49, C60	MURATA	GRM235Y5V106Z025
75	8	2.74K 1/8W 1% 1206	R140-147	DALE	CRCW12062741FRT1

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
76	20	5.49K 1/8W 1% 1206	R7, R15-16, R21, R25, R28, R31, R34, R37, R40, R43, R46, R48, R51, R54, R57, R59-62	PANASONIC	ERJ-8ENF5491V
77	8	1.65K 1/8W 1% 1206	R23, R26, R29, R32, R35, R38, R41, R44	PANASONIC	ERJ-8ENF1651V
78	10	10uF 16V 20% CAP002 ELEC	CT1-9, CT12	DIG01	PCE3062TR-ND
79	2	68uF 25V 20% CAP003 ELEC	CT10-11	PANASONIC	EEV-FC1E680P
80	1	10uH 47 +/-20 IND001	L1	DIG01	445-1202-2-ND
81	8	0.00 100MW 5% 805	R9, R12, R79-80, R126, R151, R192-193	VISHAY	CRCW0805 0.0 RT1
82	1	190 100MHZ 5A FER002	FER3	MURATA	DLW5BSN191SQ2
83	8	3.32K 100MW 1% 805	R24, R27, R30, R33, R36, R39, R42, R45	DIG01	P3.32KCCTR-ND
84	4	1.2K 1/10W 5% 805	R155-158	DALE	CRCW08051201FRT1
85	9	10UF 6.3V 10% 805	C26, C40, C50-52, C84, C145, C184-185	AVX	080560106KAT2A
86	3	6.04K 100MW 1% 805	R65, R148-149	DIGIKEY	311-6.04KCCT-ND
87	7	0.1UF 10V 10% 402	C41, C128-129, C136, C140, C142, C144	AVX	0402ZD104KAT2A

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
88	5	0.01UF 16V 10% 402	C134, C138, C147, C149, C151	AVX	0402YC103KAT2A
89	8	1000PF 50V 5% 402 CERM	C130, C135, C137, C139, C143, C146, C150, C154	AVX	04025C102JAT2A
90	2	64.9K 1/10W 1% 805	R67, R87	VISHAY INTERTEC	CRCW08056492FRT1
91	2	210K 1/4W 1% 805	R69, R88	VISHAY INTERTEC	CRCW08052103FRT1
92	1	1A SK12 DO-214AA SCHOTTKY	D3	MCC	SK12
93	1	107 1/10W 1% 805	R112	YAGEO	9C08052A1070FKHFT
94	1	249 1/10W 1% 805	R63	YAGEO	9C08052A2490FKHFT
95	1	1K 1/8W 5% 1206	R106	DALE	CRCW1206-102JRT1
96	1	100K 1/8W 5% 1206	R73	AVX	CR1206-1003FRT1
97	2	22 1/8W 5% 1206	R103-104	DALE	CRCW1206220JRT1
98	12	270 1/8W 5% 1206	R138-139, R153-154, R177-184	AVX	CR32-271J-T
99	2	RED-SMT LED001 GULL-WING	LED9, LED12	PANASONIC	LN1261C
100	1	GREEN-SMT LED001 GULL-WING	LED10	PANASONIC	LN1361C
101	8	604 1/8W 1% 1206	R127-134	DALE	CRCW12066040FRT1

Ref.	#	Description	Reference Designator	Manufacturer	Part Number
102	4	1uF 25V 20% A TANT -55+125	CT15-18	PANASONIC	ECS-T1EY105R
103	2	ADG774A QSOP16 QUICKSWITCH-257	U30-31	ANALOG DEV.	ADG774ABRQ
104	1	IDC 2X1 IDC2X1 GOLD	P1		
105	1	IDC 3X2 IDC3X2	P2	BERG	54102-T08-03
106	1	IDC 7X2 IDC7X2 HEADER	P5	BERG	54102-T08-07
107	1	IDC 13X2 IDC13X2	P3	BERG	54102-T08-13
108	1	2.5A RESETABLE FUS001	F1	RAYCHEM CORP.	SMD250-2
109	1	3.5MM STEREO_JACK CON001	J6	SHOGYO	SJ-0359AM-5

ADSP-21364 EZ-KIT Lite Schematic

DNP = Do Not Populate

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
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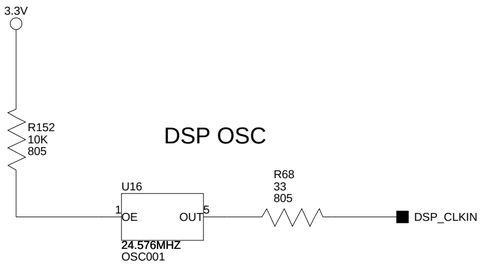
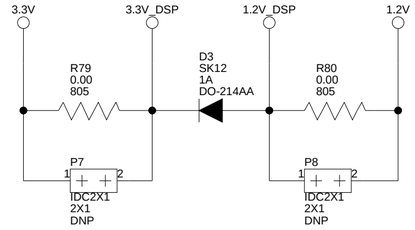
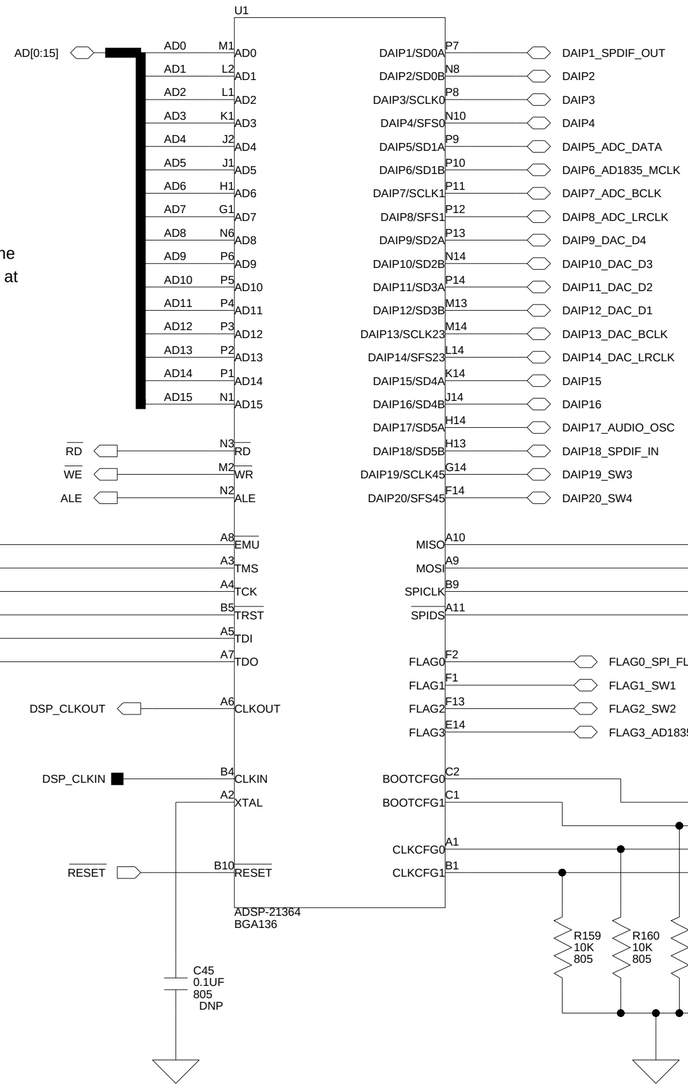
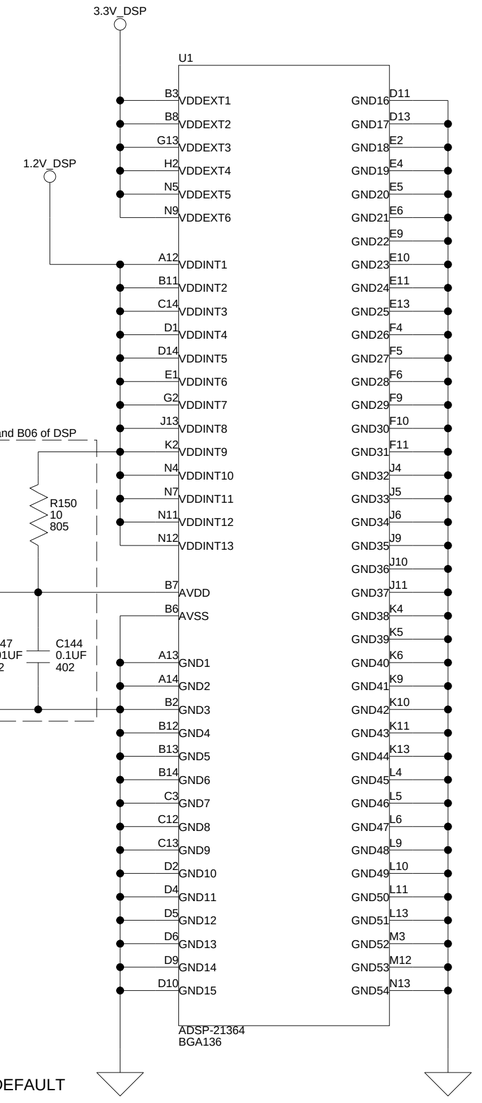
Title	ADSP-21364 EZ-KIT Lite TITLE		
Size C	**Board No.** A0190-2004		**Rev** 1.1
Date 8-25-2004_10:08		**Sheet** 1 **of** 12	





When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com



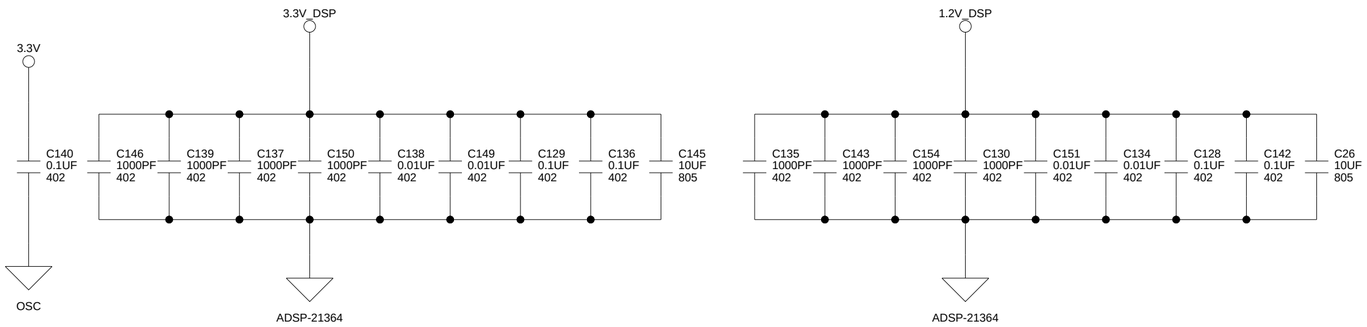


SW10: BOOT/CLOCK RATIO SELECT
(Default: 1=OFF, 2=ON, 3=OFF, 4=OFF)

1	2	
BOOTCFG0	BOOTCFG1	BOOTMODE
OFF	OFF	SPI SLAVE BOOT
ON	OFF	SPI MASTER BOOT
OFF	ON	PARALLEL PORT BOOT
ON	ON	RESERVED
3	4	CLOCK RATIO
CLKCFG0	CLKCFG1	CORE:CLKIN
OFF	OFF	6:1
ON	OFF	32:1
OFF	ON	16:1
ON	ON	RESERVED

DEFAULT

DEFAULT



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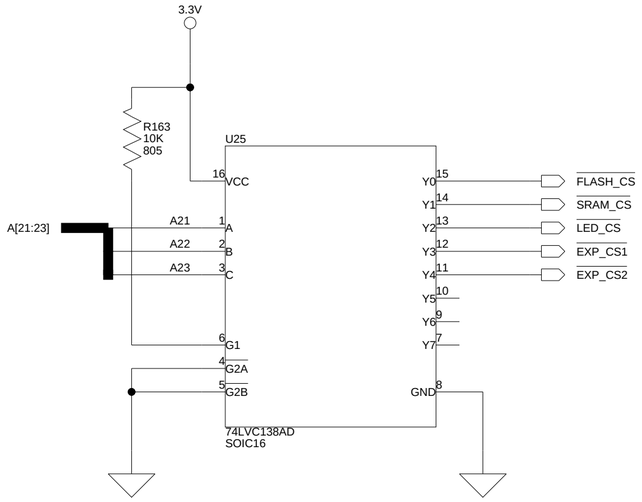
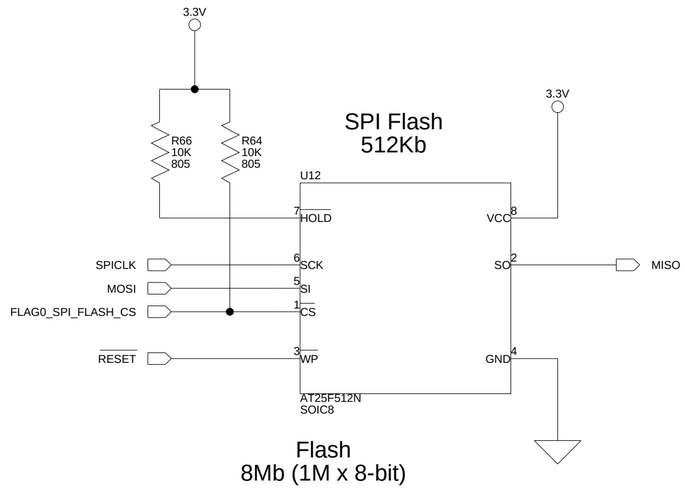
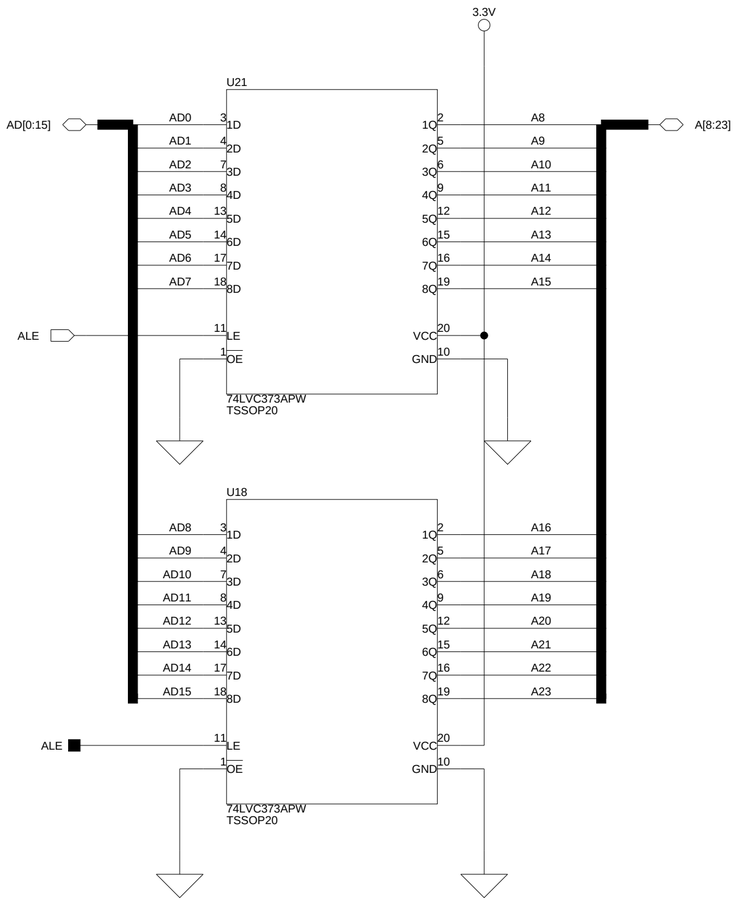
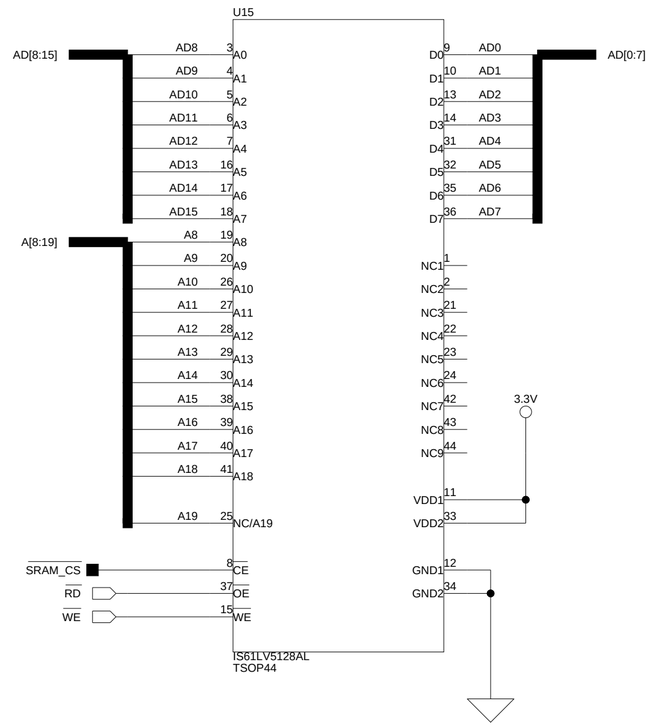
Title	ADSP-21364 EZ-KIT Lite DSP		
Size C	Board No. A0190-2004		Rev 1.1
Date 7-8-2004_8:55		Sheet 2 of 12	

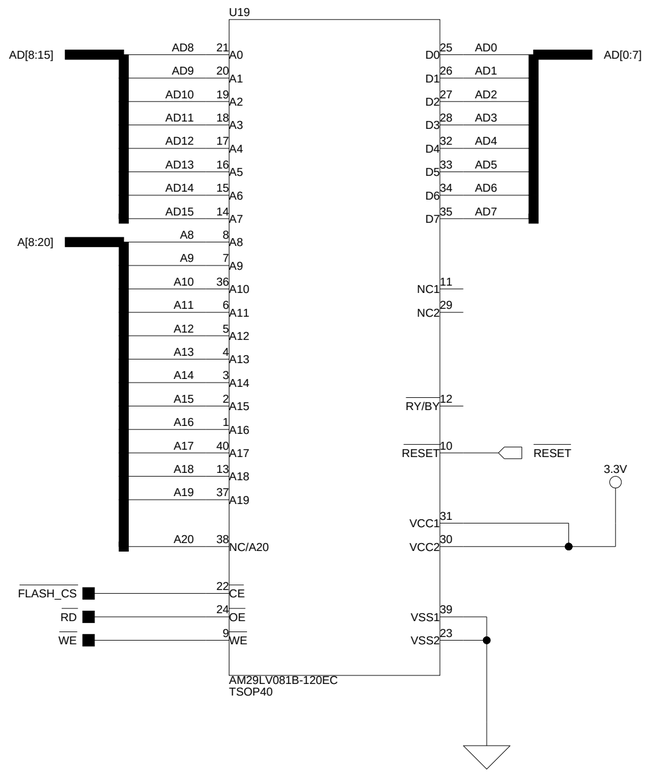


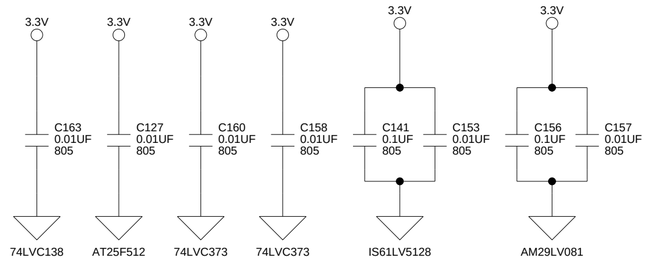
VALID DSP ADDRESS		BANK END	A23	A22	A21	BANK	DEVICE
START	END	ADDRESS					
1A0 0000	X	1FF FFFF	1	-	-	-	NONE
180 0000	X	19F FFFF	1	0	0	Y4	EXPANSION INTERFACE CS 2
160 0000	X	17F FFFF	0	1	1	Y3	EXPANSION INTERFACE CS 1
140 0000	140 0000	15F FFFF	0	1	0	Y2	LEDs
120 0000	127 FFFF	13F FFFF	0	0	1	Y1	SRAM
100 0000	10F FFFF	11F FFFF	0	0	0	Y0	FLASH











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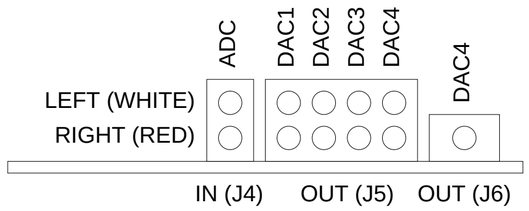
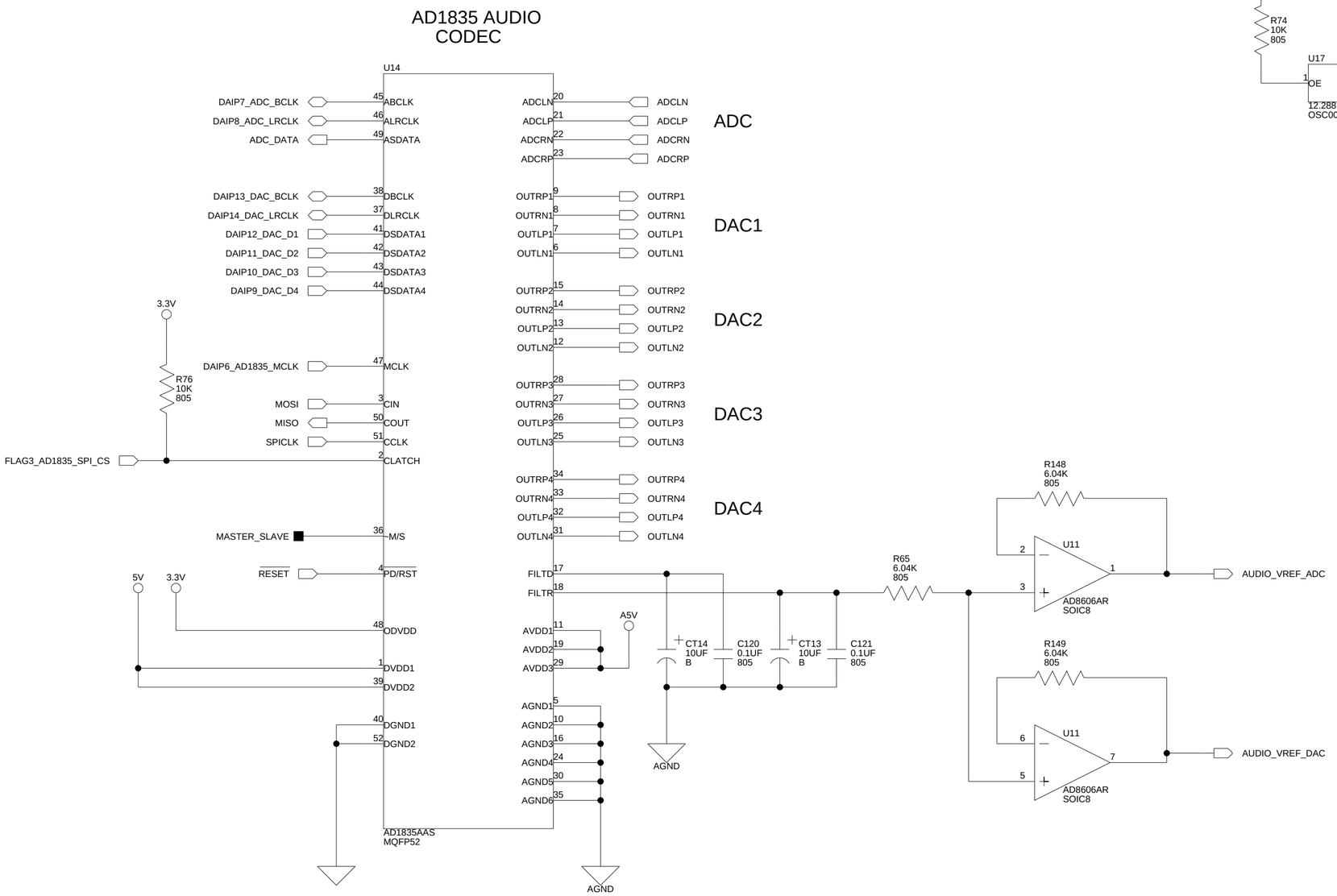
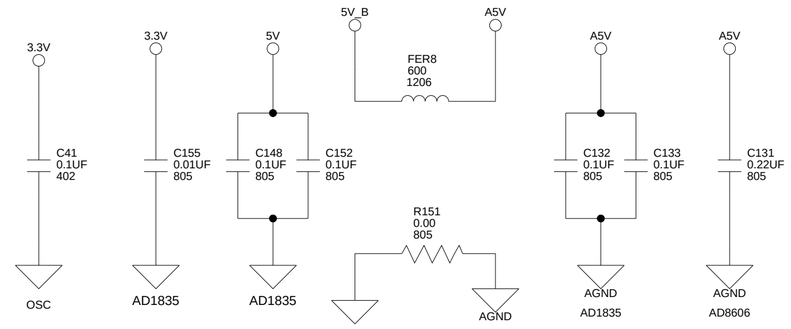
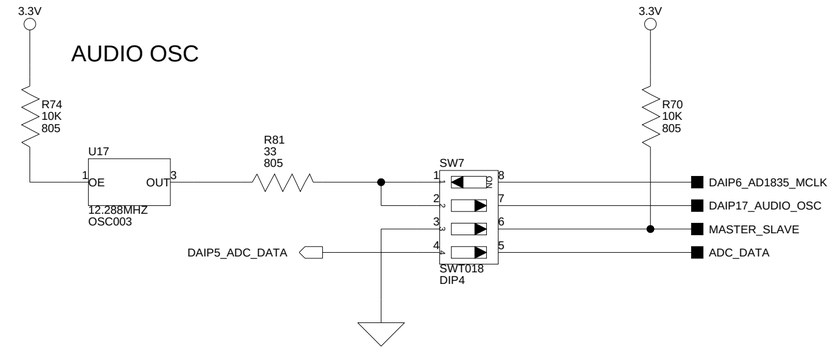
PH: 1-800-ANALOGD

Title	ADSP-21364 EZ-KIT Lite MEMORY		
Size C	**Board No.** A0190-2004		**Rev** 1.1
Date 6-22-2004_10:11		**Sheet** 3 **of** 12	



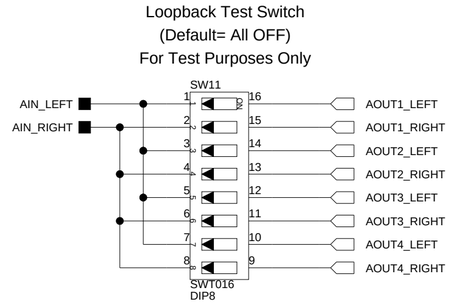






SW7: CODEC SETUP SWITCH
(Default: 1=OFF, 2=ON, 3=ON, 4=ON)

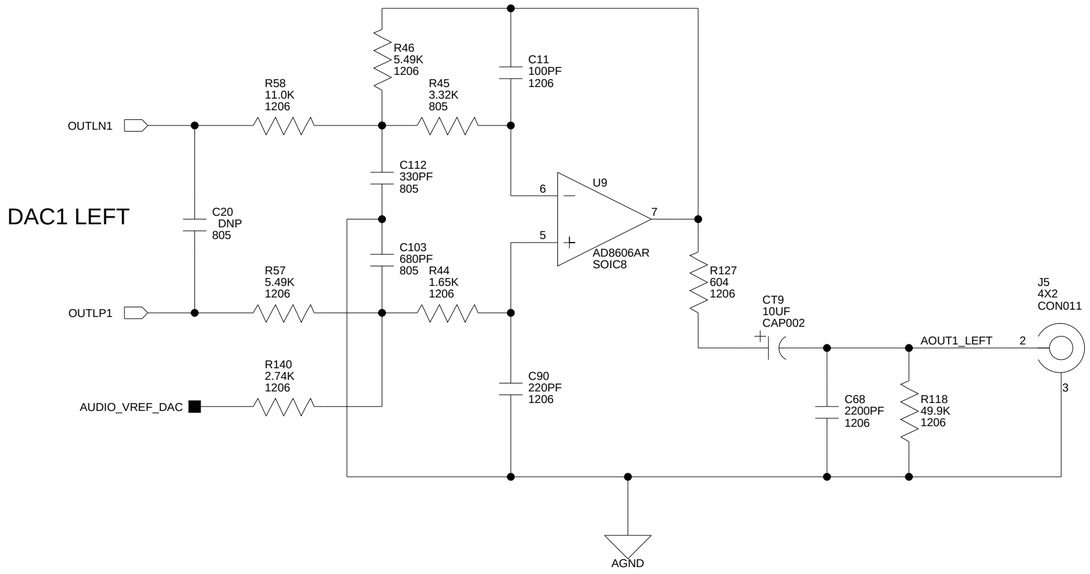
1-2	Connects or disconnects the audio oscillator depending on how the system is setup. See users manual for more information.
3	OFF = AD1835 is SLAVE ON = AD1835 is MASTER
4	Disconnects ADC_DATA signal from driving the corrisponding DAI signal. Useful if using this DAI pin for another purpose.

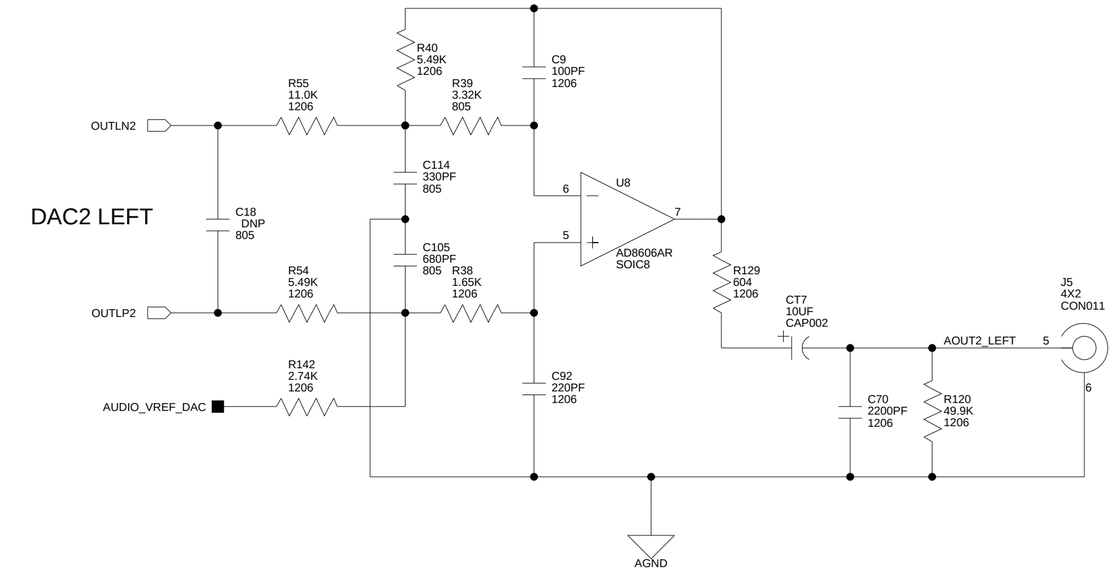


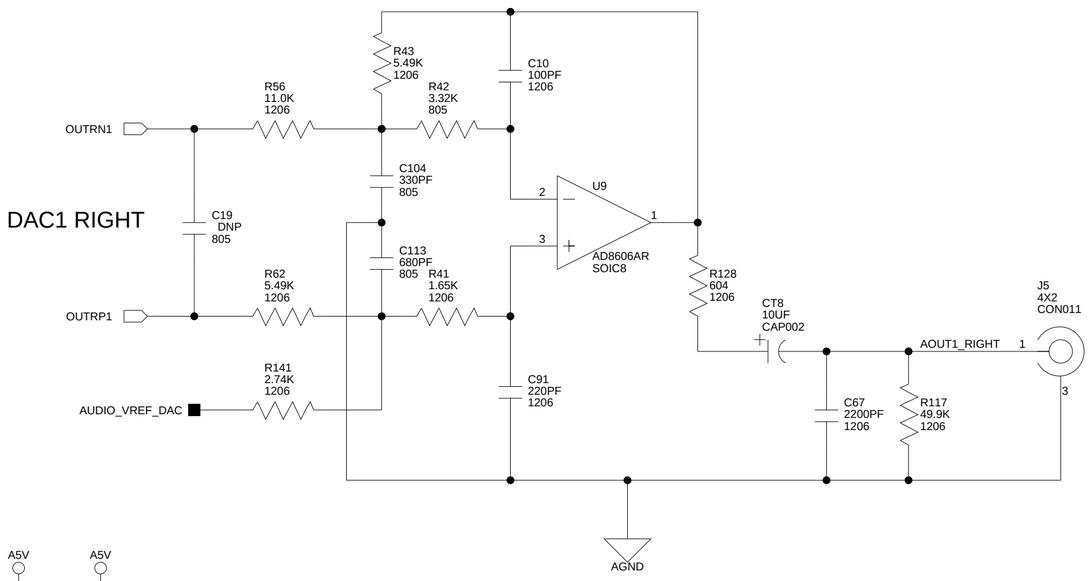
DNP = Do Not Populate

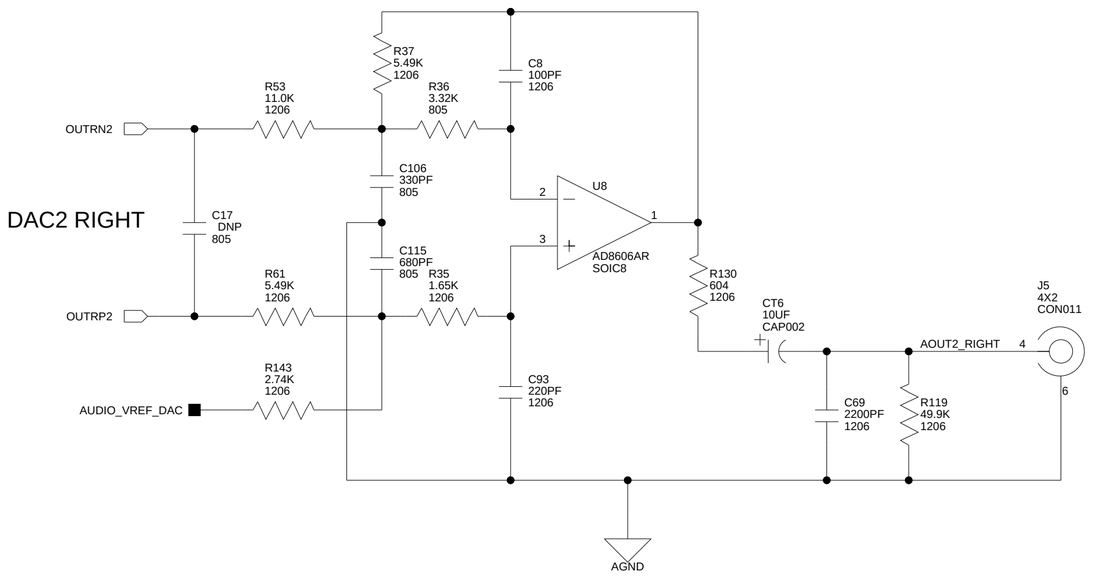
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

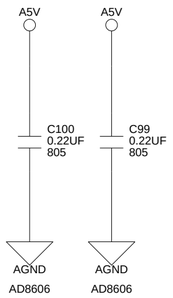
Title	ADSP-21364 EZ-KIT Lite ANALOG AUDIO	
Size C	**Board No.** A0190-2004	**Rev** 1.1
Date 6-22-2004_10:11	**Sheet** 4 **of** 12	





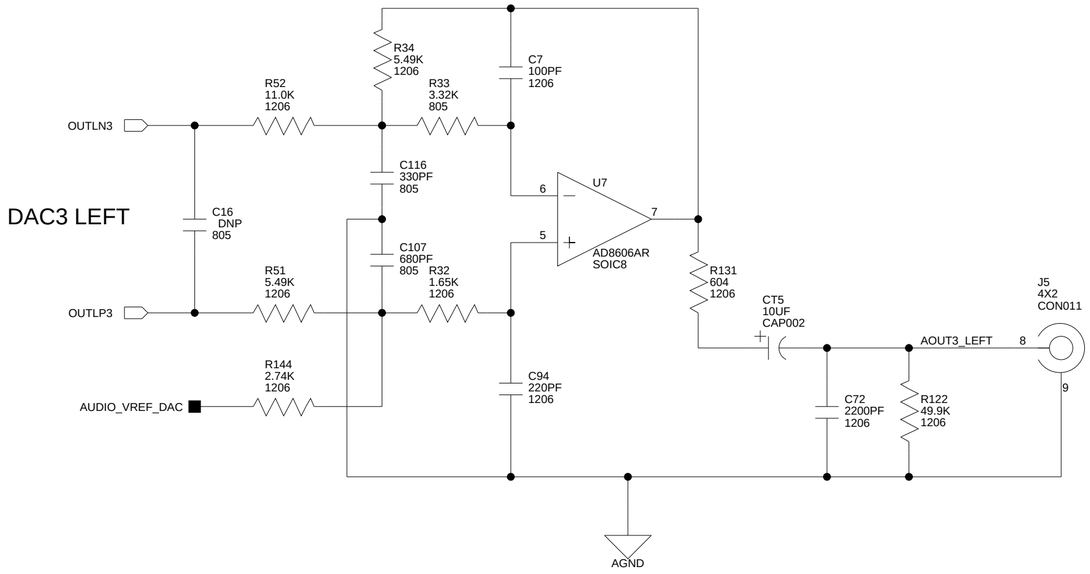


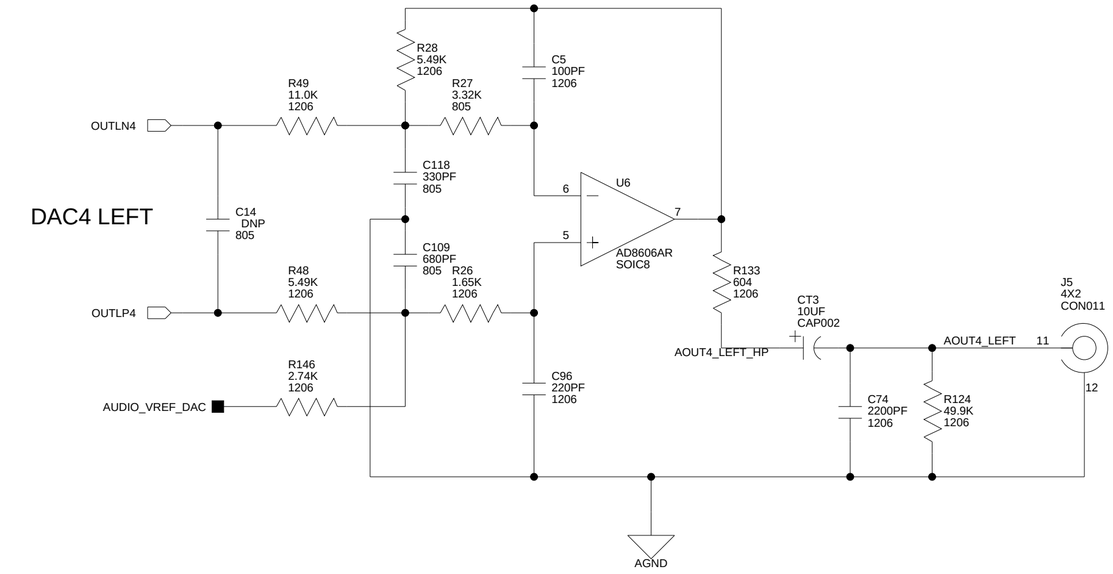


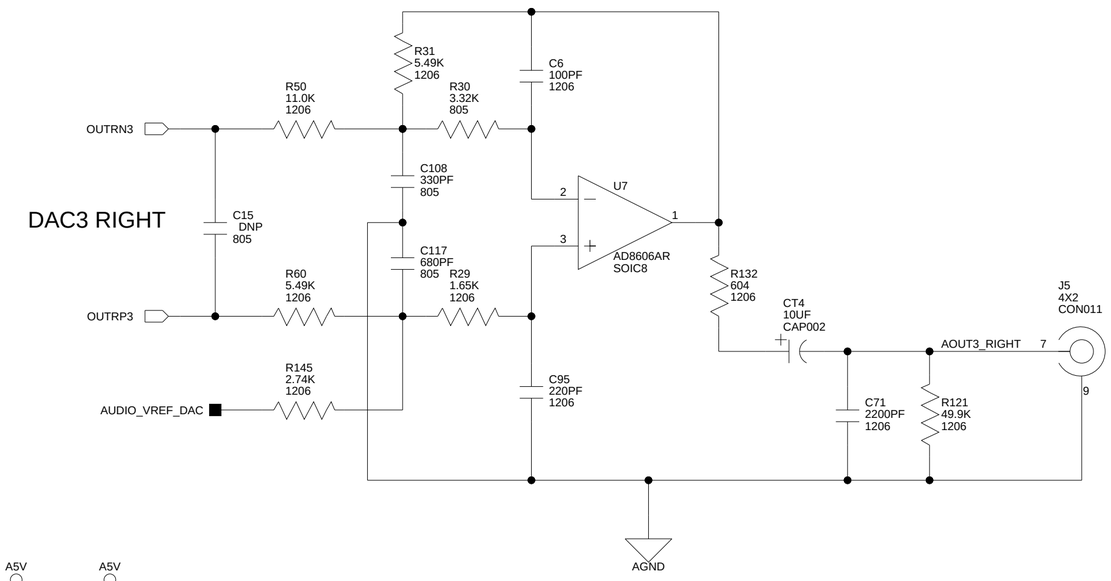


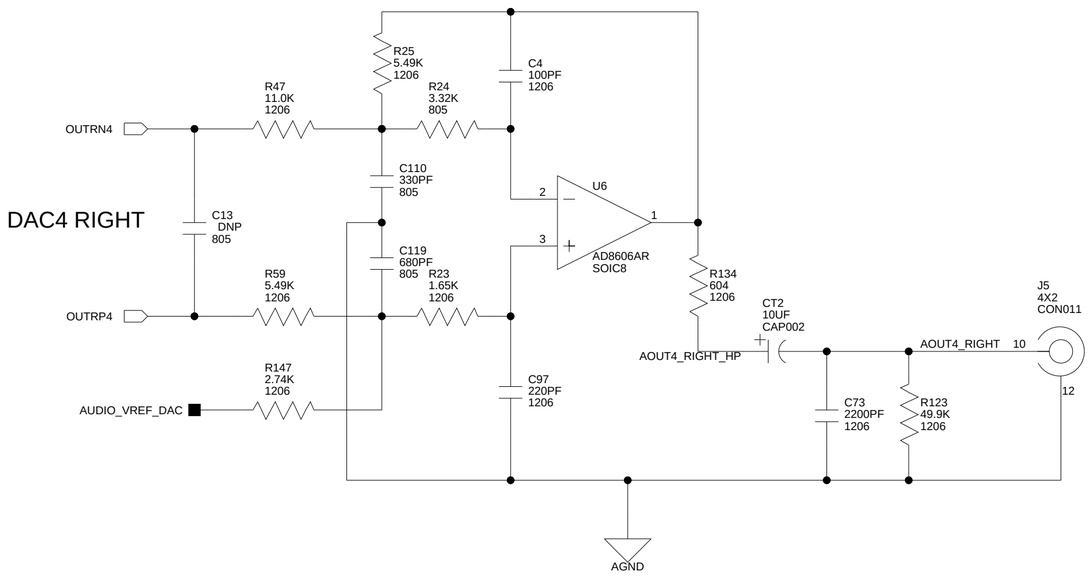
DNP = Do Not Populate

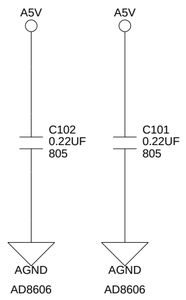
ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-21364 EZ-KIT Lite AUDIO OUT 1	
Size C	**Board No.** A0190-2004	**Rev** 1.1
Date 6-22-2004_10:11	**Sheet** 5 **of** 12	







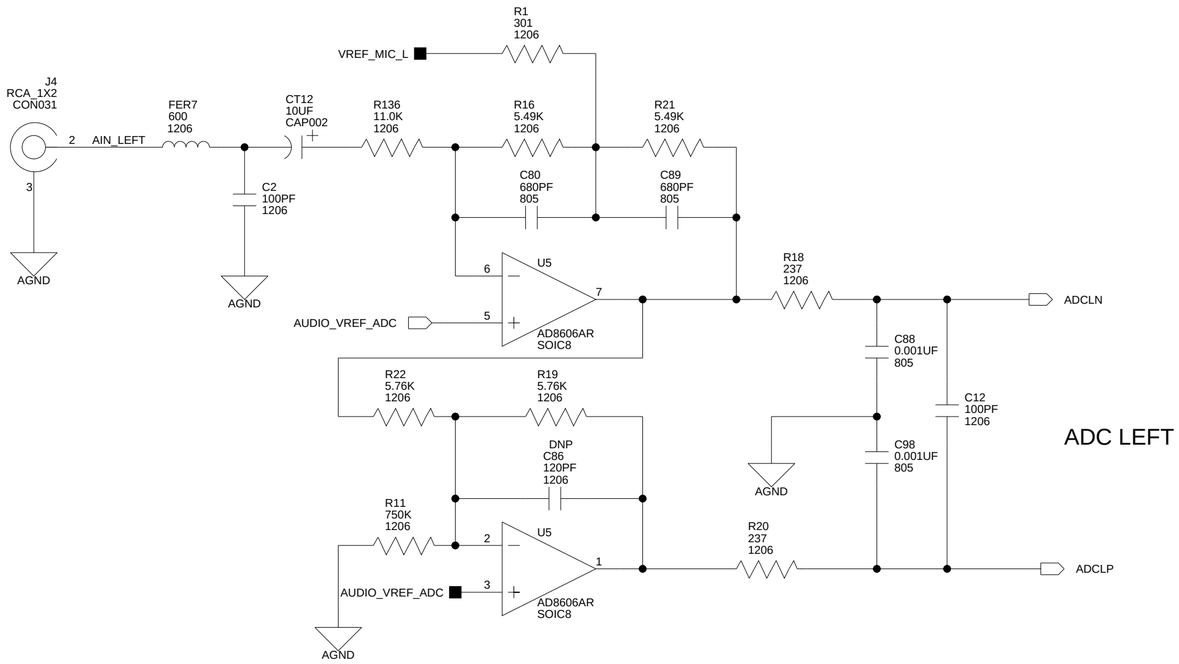




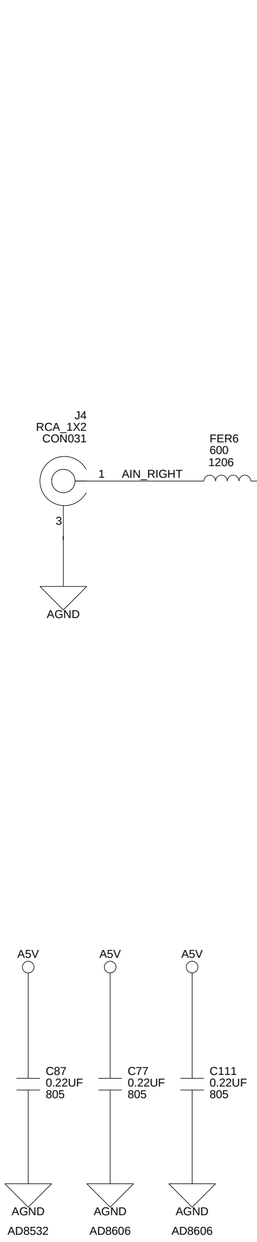
DNP = Do Not Populate

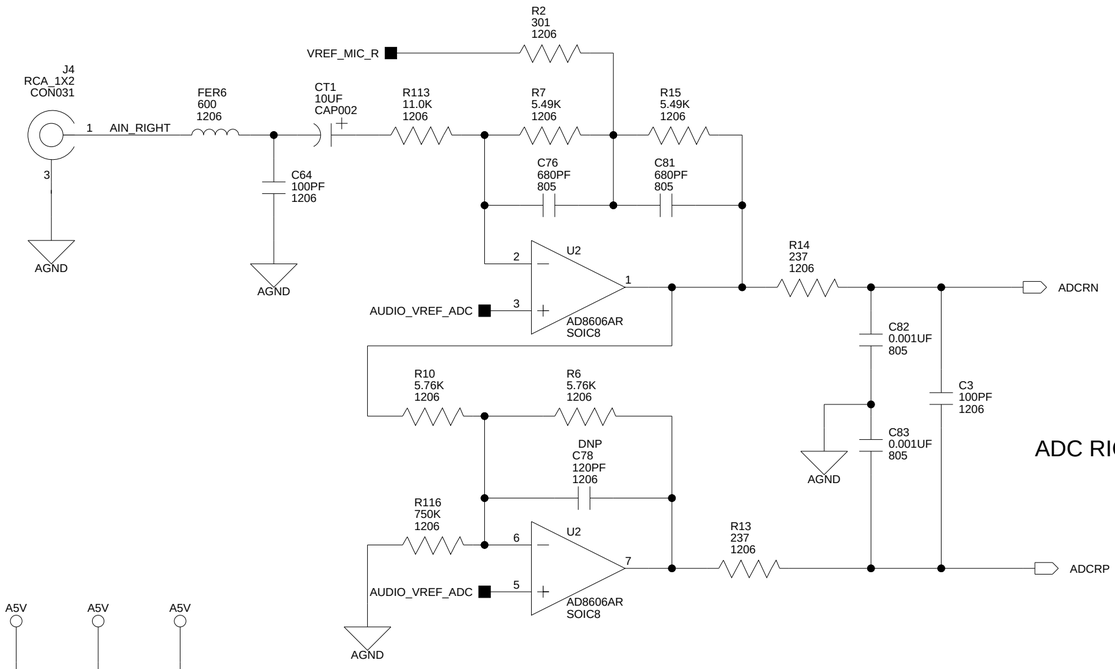
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-21364 EZ-KIT Lite AUDIO OUT 2	
Size C	**Board No.** A0190-2004	**Rev** 1.1
Date 6-22-2004_10:11	**Sheet** 6 **of** 12	



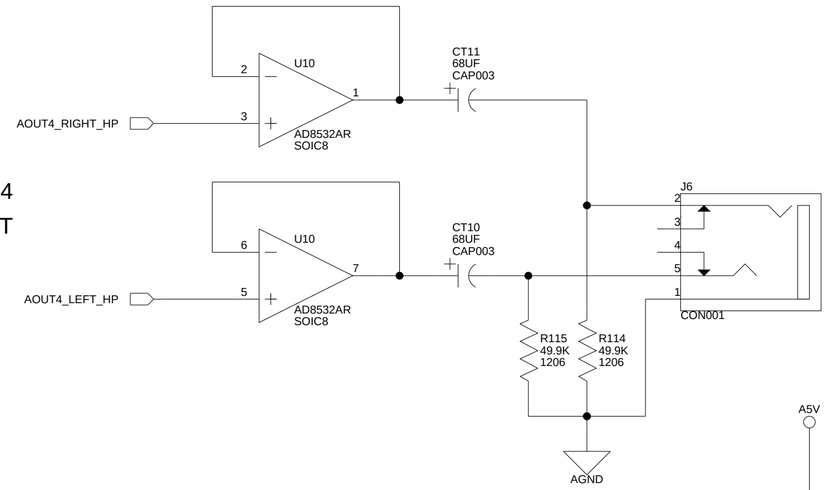
ADC LEFT

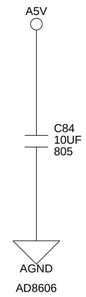


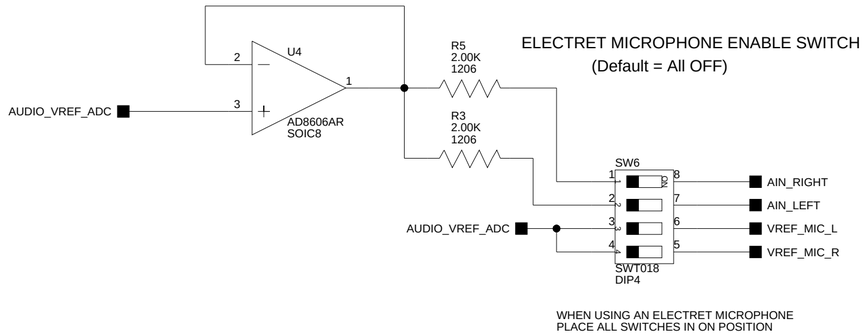


ADC RIGHT

DAC4
HEADPHONE OUT







ELECTRET MICROPHONE ENABLE SWITCH
(Default = All OFF)

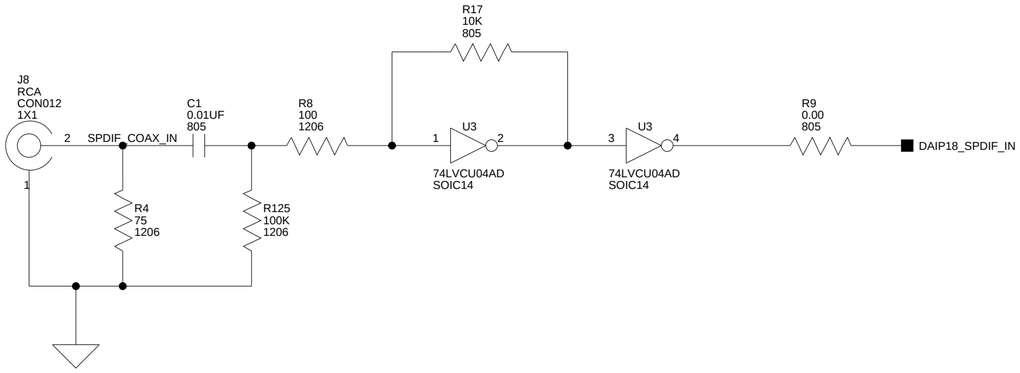
WHEN USING AN ELECTRET MICROPHONE
PLACE ALL SWITCHES IN ON POSITION

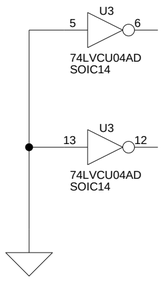
DNP = Do Not Populate

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

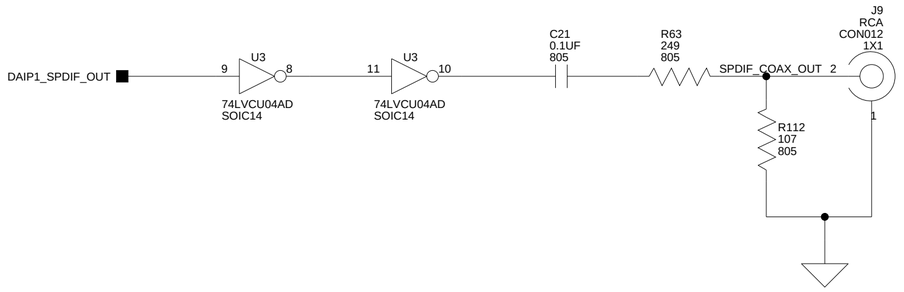
Title	ADSP-21364 EZ-KIT Lite AUDIO OUT 3	
Size: C	Board No.: A0190-2004	Rev: 1.1
Date: 6-29-2004_20:04	Sheet: 7 of 12	

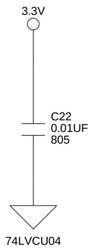
SPDIF
COAX
INPUT



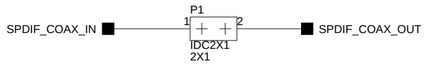


SPDIF
COAX
OUT





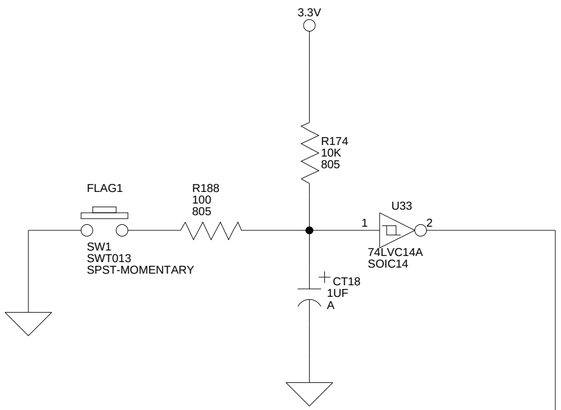
HEADER FOR LOOPBACK TEST ONLY

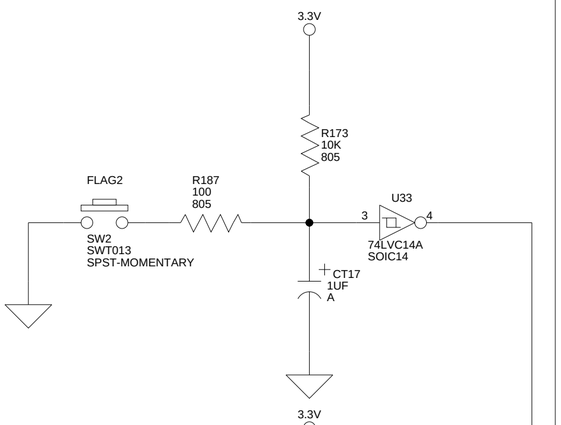


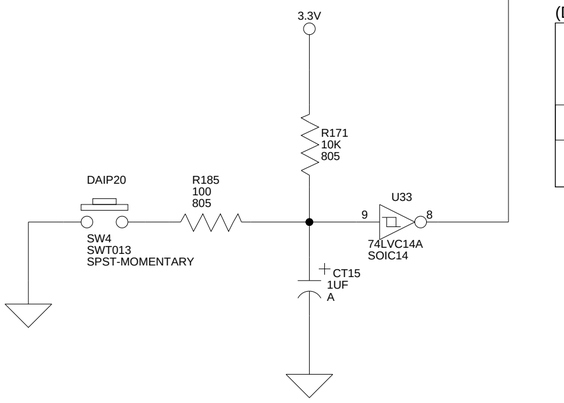
DNP = Do Not Populate

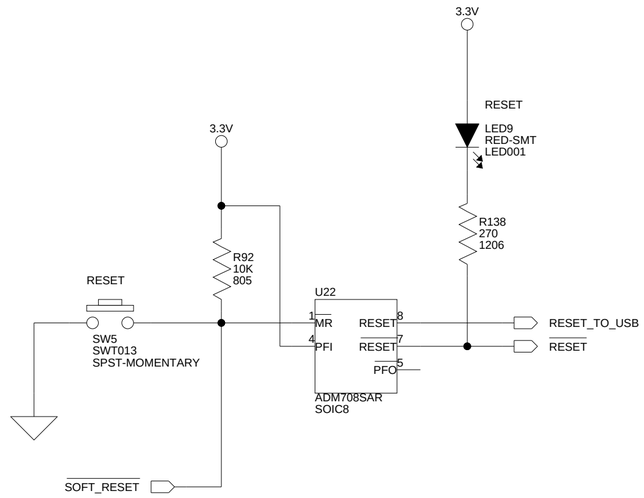
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

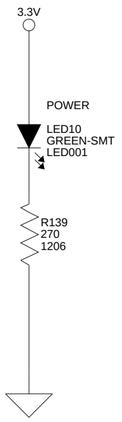
Title	ADSP-21364 EZ-KIT Lite SPDIF CONNECTORS		
Size C	**Board No.** A0190-2004		**Rev** 1.1
Date 9-8-2004_8:15		**Sheet** 8 **of** 12	

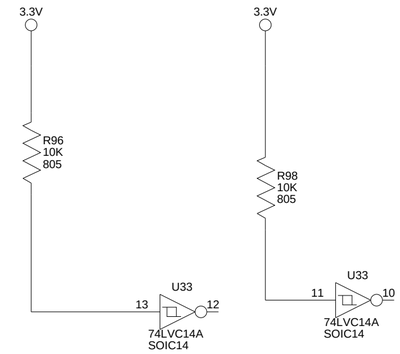


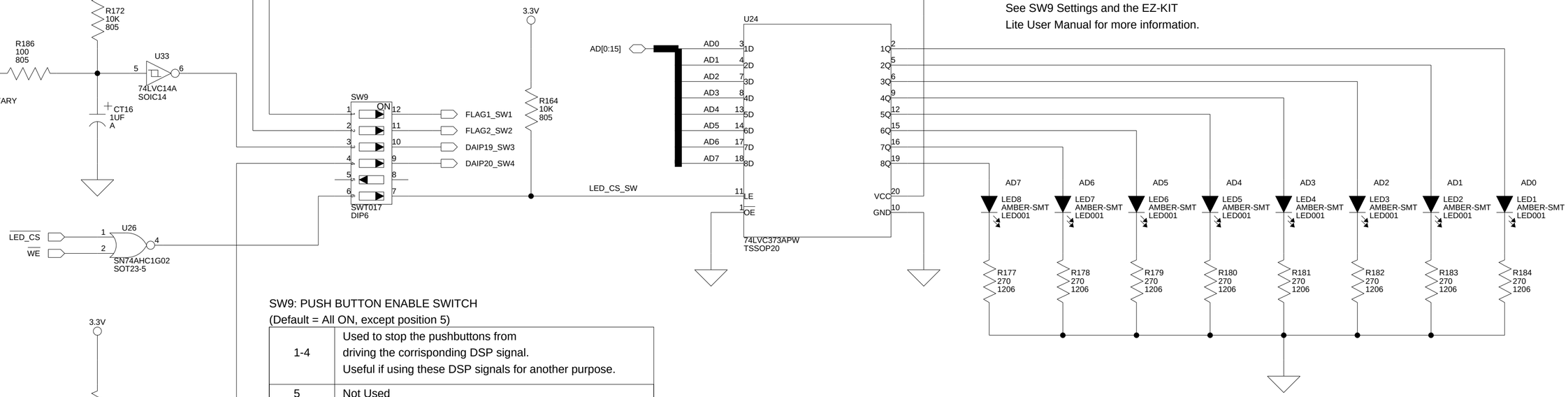








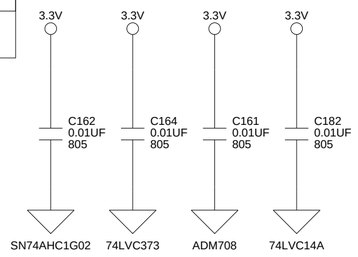




LEDs can be accessed as a memeory address,
or directly as flags depending on the DSP settings.
See SW9 Settings and the EZ-KIT
Lite User Manual for more information.

SW9: PUSH BUTTON ENABLE SWITCH
(Default = All ON, except position 5)

1-4	Used to stop the pushbuttons from driving the corrisponding DSP signal. Useful if using these DSP signals for another purpose.
5	Not Used
6	OFF = LEDs function as flags ON = LEDs are accessed at a memory address

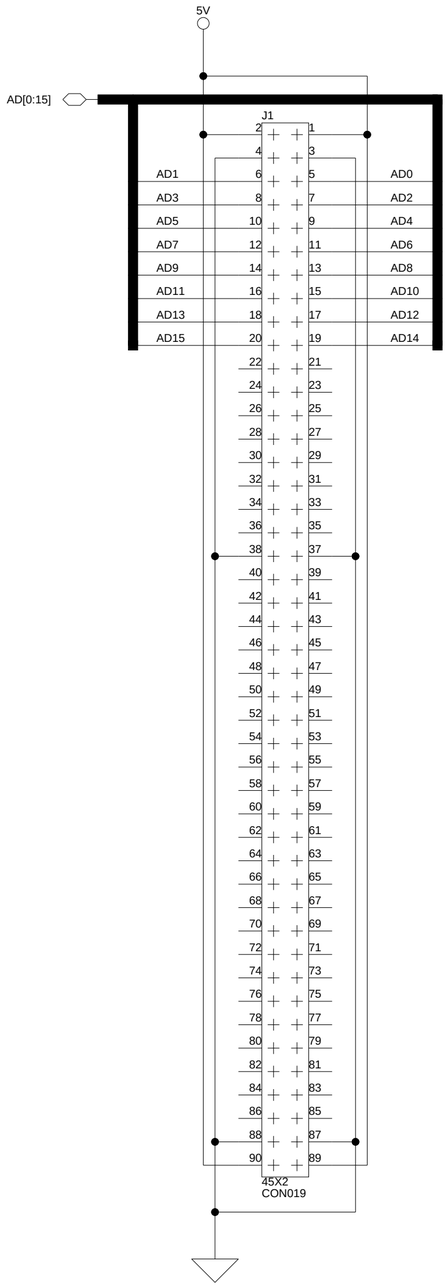


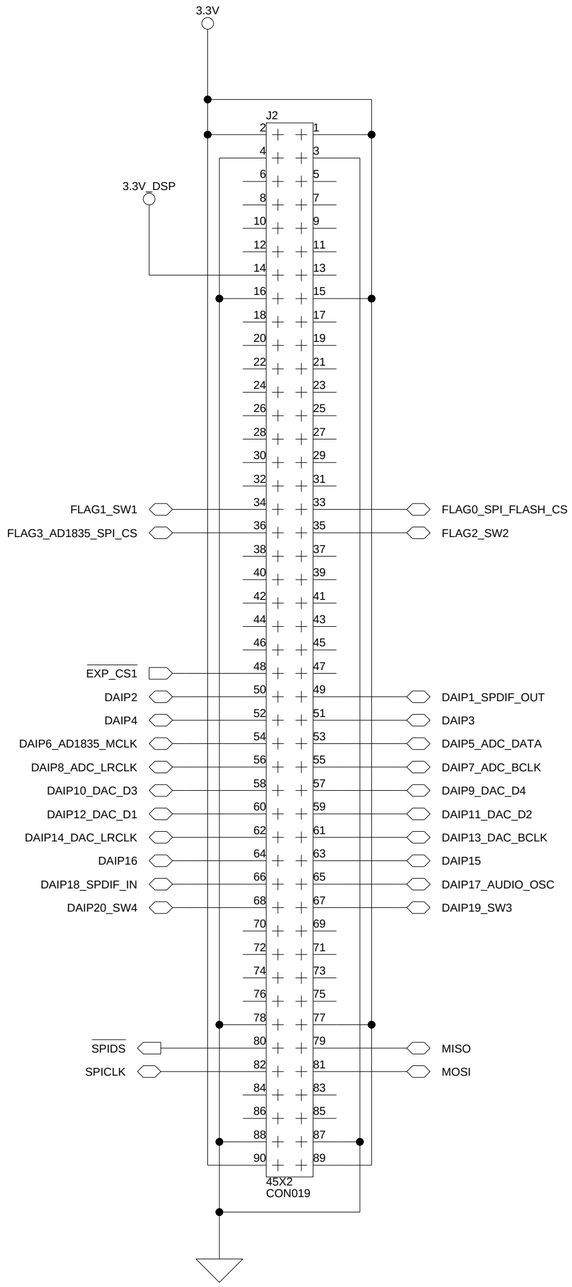
DNP = Do Not Populate

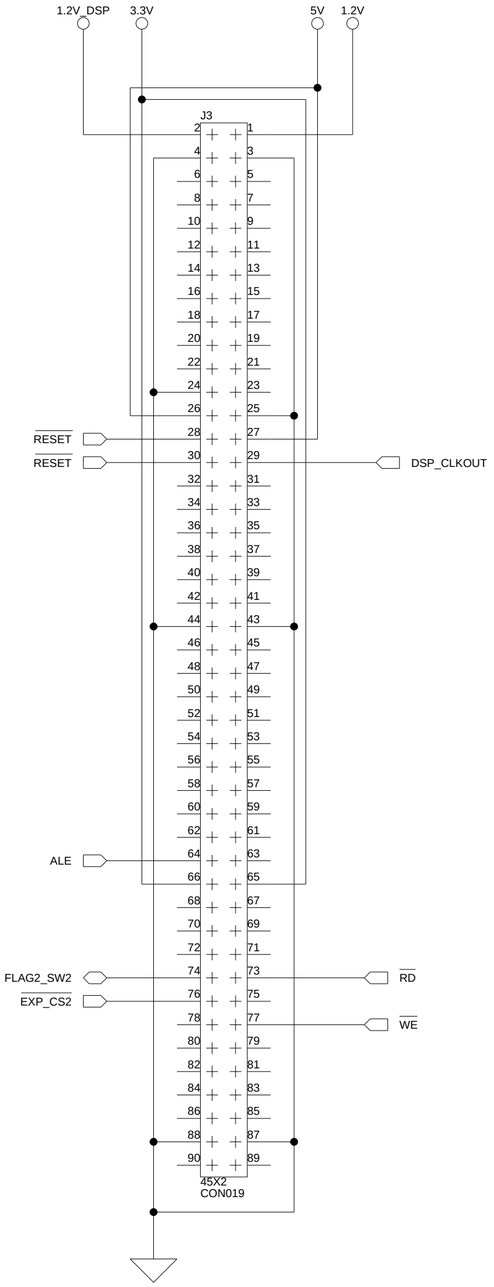
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-21364 EZ-KIT Lite USER IO/RESET	
Size C	Board No. A0190-2004	Rev 1.1
Date 6-22-2004_11:17	Sheet 8 of 11	

EXPANSION INTERFACE (TYPE A)



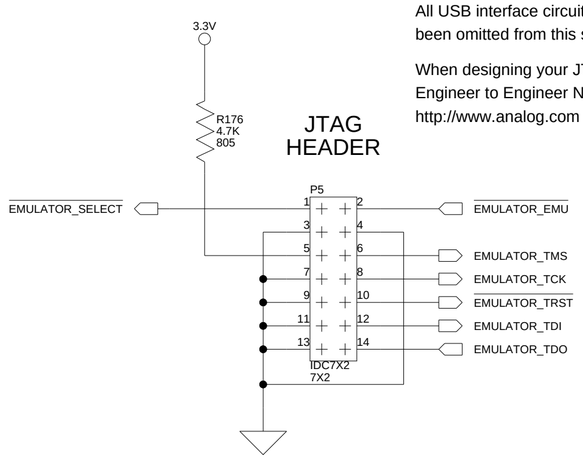




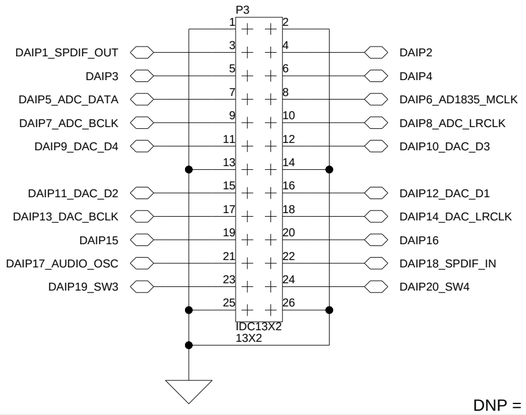
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com

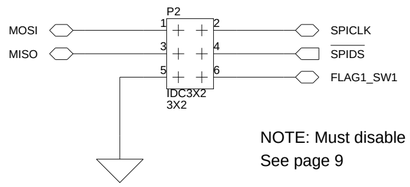
JTAG HEADER



DAI HEADER



SPI HEADER



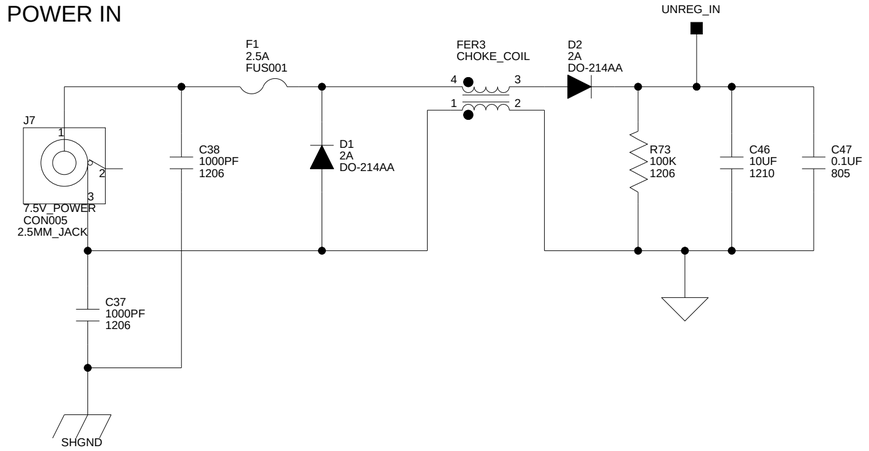
NOTE: Must disable SW1 when using this pin as SPI select.
See page 9

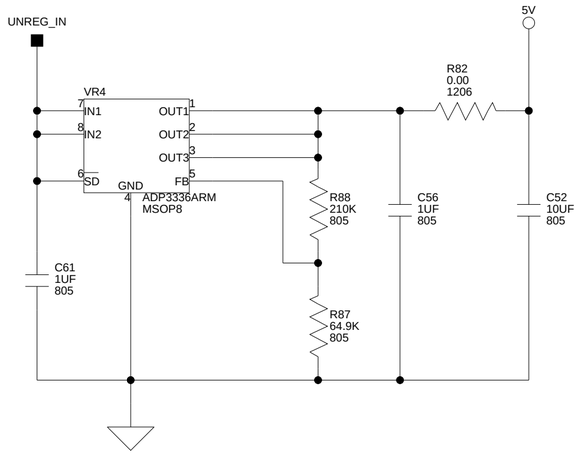
DNP = Do Not Populate

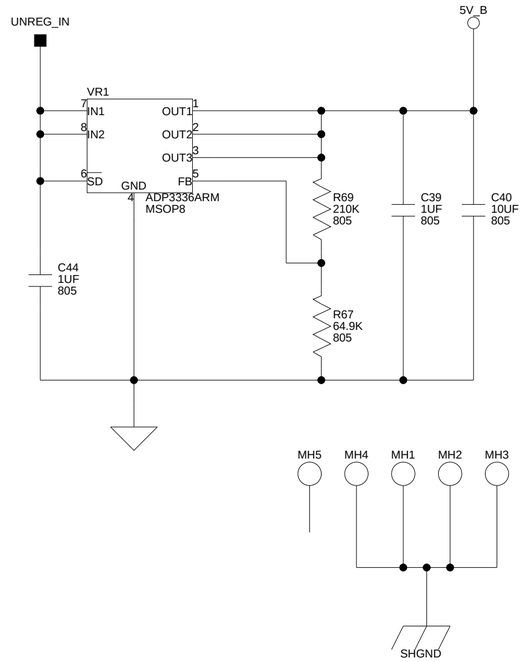
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

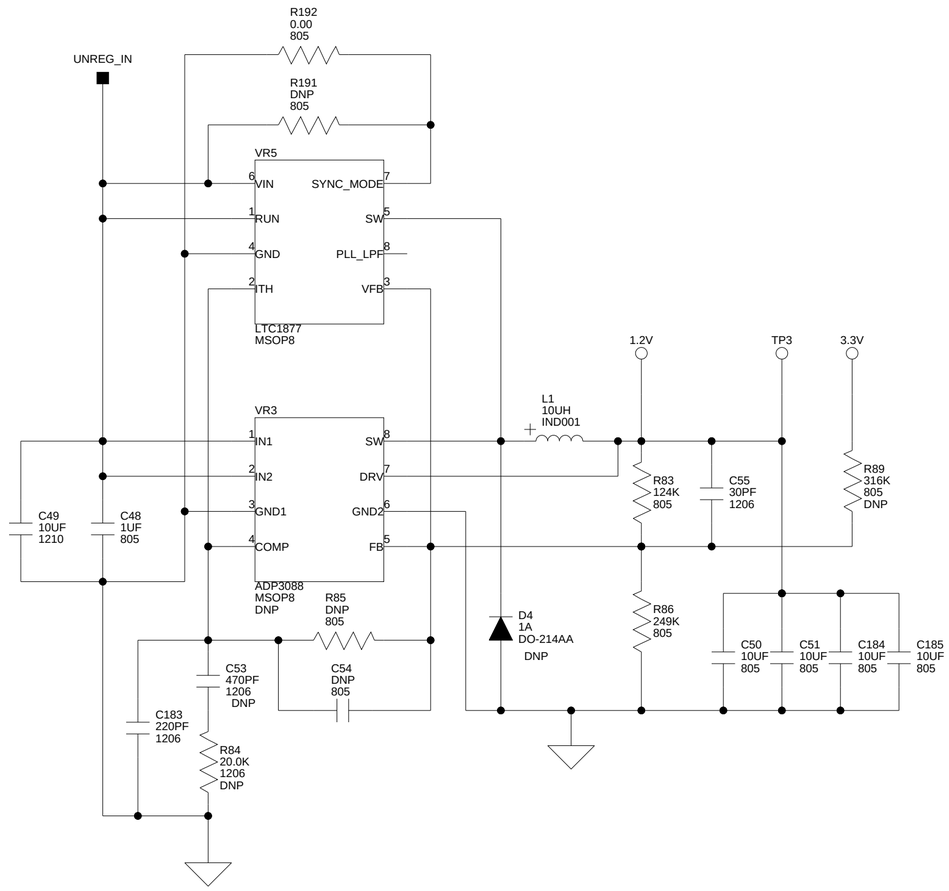
Title	ADSP-21364 EZ-KIT Lite CONNECTORS		
Size C	**Board No.** A0190-2004		**Rev** 1.1
Date 6-29-2004_19:25		**Sheet** 10 **of** 12	

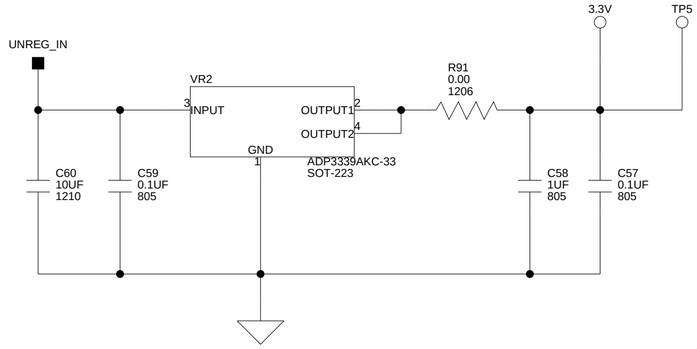
POWER IN

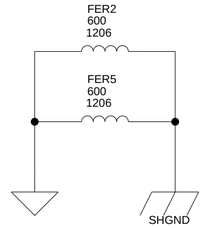


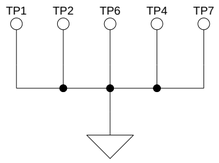












REFERENCE DESIGNATOR	ADP3088 POPULATION OPTION	LTC1877 POPULATION OPTION (DEFAULT)
R89	316K	DNP
VR3	ADP3088	DNP
VR5	DNP	LTC1877
R191	DNP	DNP
R192	DNP	0
D4	POP	DNP
R83	53.6K	124K
R86	221K	249K
C53	470pF	DNP
R84	20K	DNP
C183	10pF	220pF
C55	470pF	30pF

DNP = Do Not Populate

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-21364 EZ-KIT Lite POWER	
Size C	**Board No.** A0190-2004	**Rev** 1.1
Date 6-30-2004_16:39	**Sheet** 11 **of** 12	

I INDEX